

GL Silicon N-Channel Power MOSFET

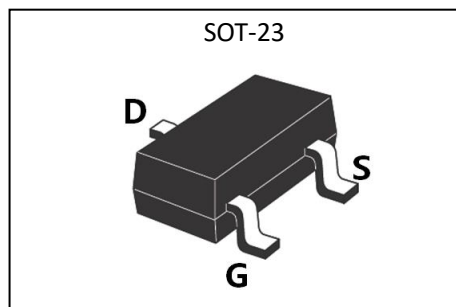
General Description

The GL3400K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the RoHS standard.

V_{DSS}	30	V
I_D	5.8	A
P_D	0.35	W
$R_{DS(ON)MAX}$	30	m Ω

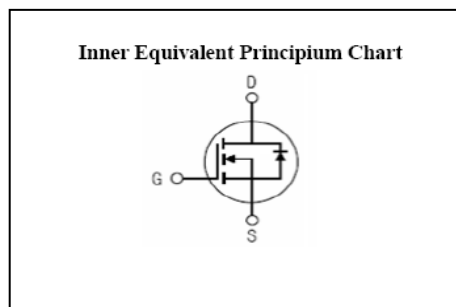
Features

- $R_{DS(ON)} < 30m\Omega$ @ $V_{GS}=10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Absolute (Tc= 25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	30	V
I_D	Continuous Drain Current	5.8	A
I_{DM}	Pulsed Drain Current	30	A
V_{GS}	Gate-to-Source Voltage	± 12	V
P_D	Power Dissipation	0.35	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}C$

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient ^{a2}	357	$^{\circ}C/W$

**GL Silicon N-Channel Power MOSFET****Electrical Characteristics** (Tc= 25°C unless otherwise specified)**OFF Characteristics**

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =24V, V _{GS} = 0V, T _a =25°C	--	--	1.0	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} = +12V	--	--	0.1	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} = -12V	--	--	-0.1	μA

ON Characteristics^{a3}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} = 10V, I _D =5.8A	--	--	30	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.7	--	1.4	V

Pulse width tp≤380μs, δ≤2%

Dynamic Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =5A	8	--	--	S
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V f=1.0MHz	--	--	1050	pF
C _{oss}	Output Capacitance		--	99	--	
C _{rss}	Reverse Transfer Capacitance		--	77	--	

Resistive Switching Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	V _{DD} = 10V, R _L =2.7Ω V _{GS} =10V, R _G =3Ω	--	--	5	ns
t _r	Rise Time		--	--	7	
t _{d(OFF)}	Turn-Off Delay Time		--	--	40	
t _f	Fall Time		--	--	6	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{SD}	Diode Forward Voltage ^{a3}	I _S =1A, V _{GS} =0V	--	--	1	V

^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2}: Surface Mounted on FR4 Board, t≤10sec.

^{a3}: Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.

^{a4}: Guaranteed by design, not subject to production

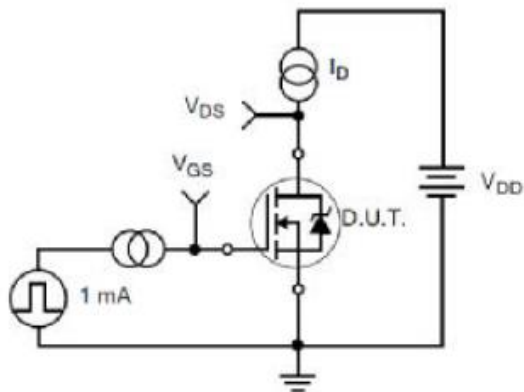
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Test Circuits


Figure 17. Gate Charge Test Circuit

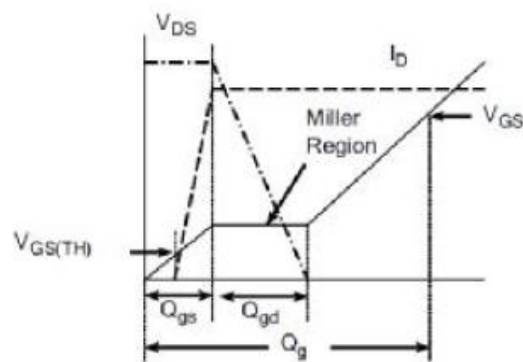


Figure 18. Gate Charge Waveform

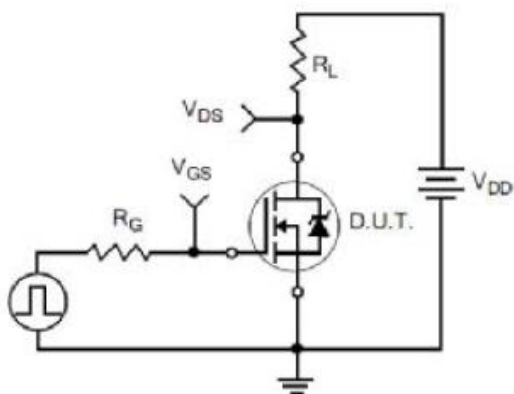


Figure 19. Resistive Switching Test Circuit

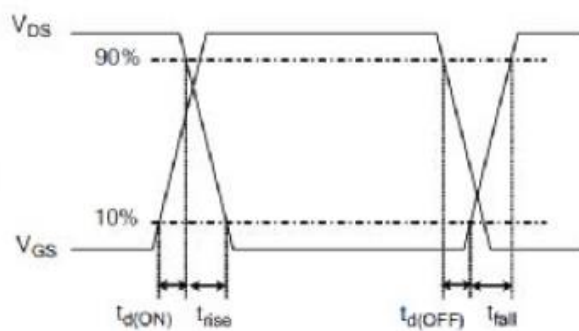


Figure 20. Resistive Switching Waveforms

Characteristics Curves

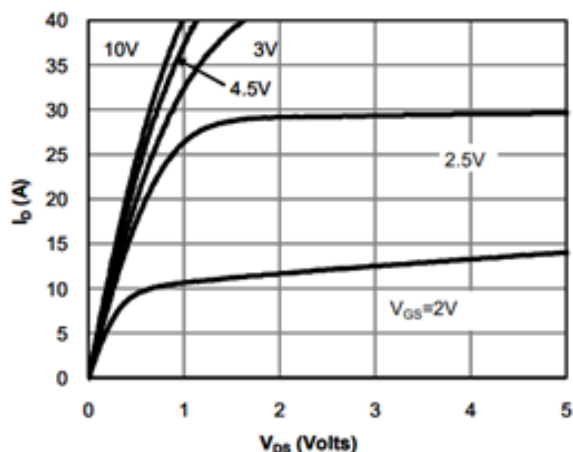


Fig 1: On-Region Characteristics (Note E)

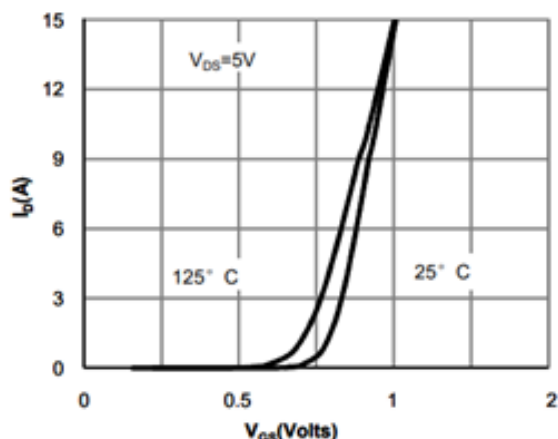


Figure 2: Transfer Characteristics (Note E)

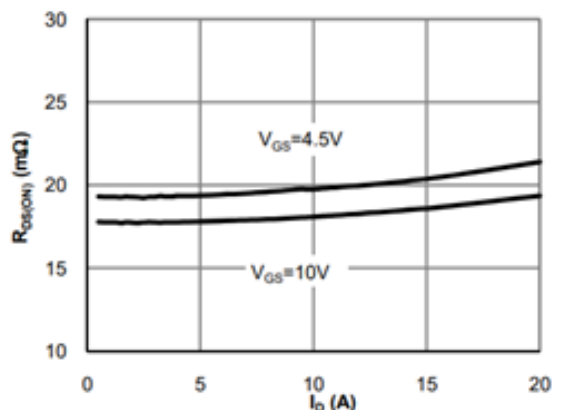


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

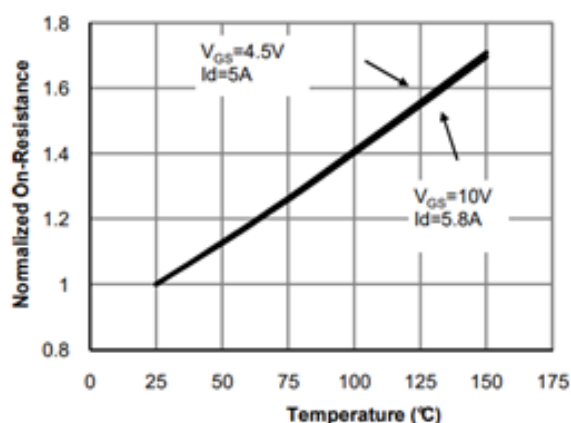


Figure 4: On-Resistance vs. Junction Temperature (Note E)

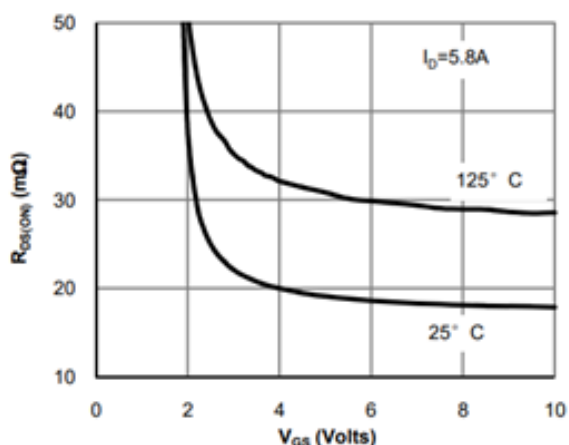


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

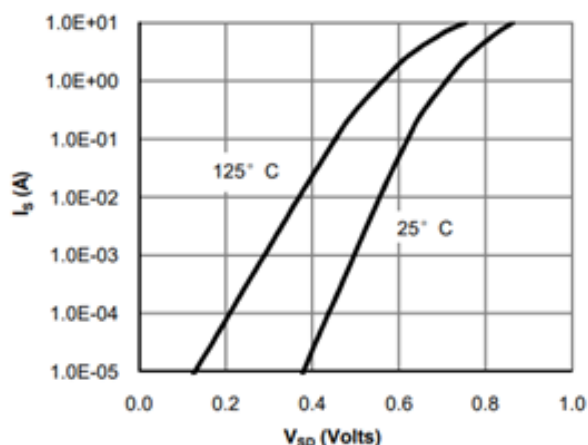


Figure 6: Body-Diode Characteristics (Note E)

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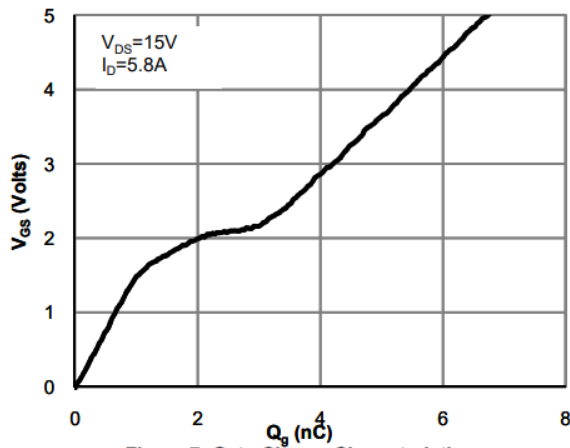


Figure 7: Gate-Charge Characteristics

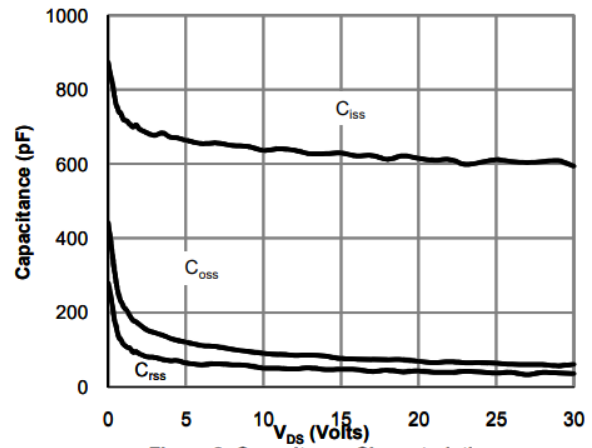


Figure 8: Capacitance Characteristics

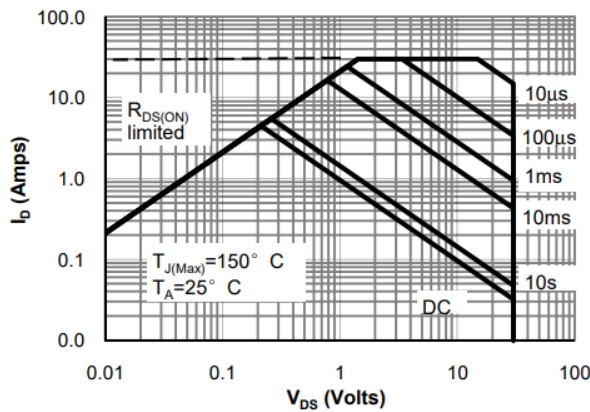


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

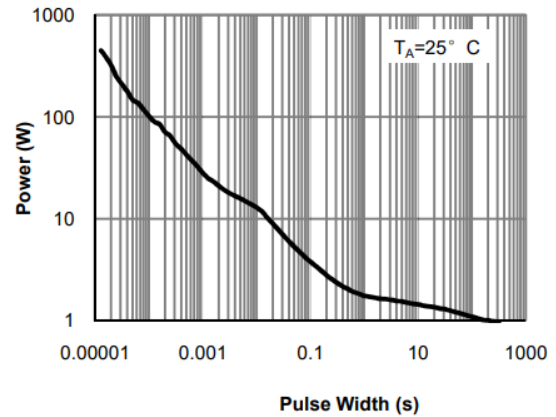


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

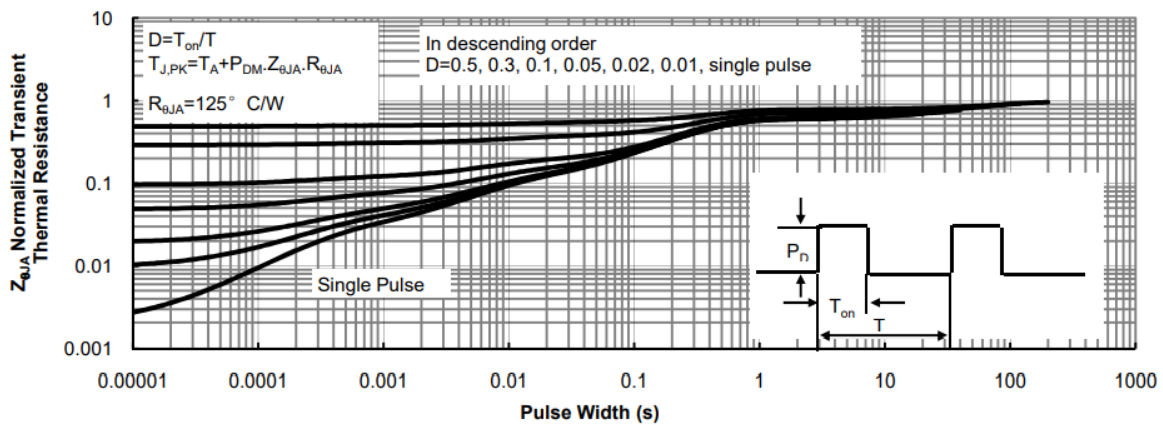


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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