

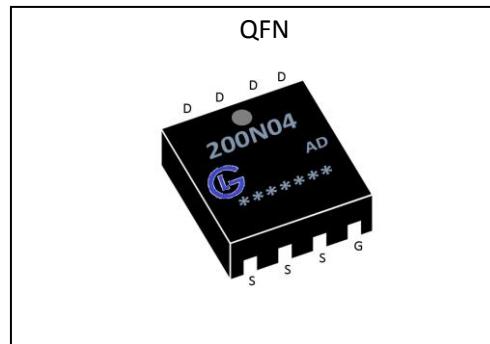
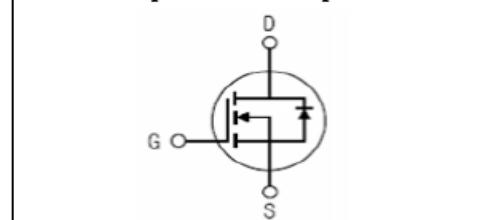
GL Silicon N-Channel Power MOSFET
General Description :

The GL200N04AD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is QFN, which accords with the RoHS standard.

V_{DSS}	40	V
I_D	200	A
P_D	114	W
$R_{DS(ON)}\text{type}$	1.0	$\text{m}\Omega$

Features :

- $R_{DS(ON)} < 1.5\text{m}\Omega$ @ $V_{GS}=10\text{V}$ (Typ1.0mΩ)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation


Inner Equivalent Principium Chart

Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	200	A
I_{DM}	Pulsed Drain Current	800	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	114	W
E_{AS}	Single pulse avalanche energy ^{a5}	238	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$



GL200N04AD

无锡光磊电子科技有限公司

GL Silicon N-Channel Power MOSFET

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu\text{A}$	40	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=40V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-0.1	μA

ON Characteristics ^{a3}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=100A$	--	1.0	1.5	$\text{m}\Omega$
$V_{GS(\text{TH})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	--	2.5	V

Pulse width $t_p \leq 380\mu\text{s}, \delta \leq 2\%$

Dynamic Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=80A$	--	160	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=20V$	--	6020	--	pF
C_{oss}	Output Capacitance	$f=1.0\text{MHz}$	--	2230	--	
C_{rss}	Reverse Transfer Capacitance		--	170	--	

Resistive Switching Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{DD}=20V, I_D=80A$	--	25	--	ns
t_r	Rise Time		--	80	--	
$t_{d(\text{OFF})}$	Turn-Off Delay Time		--	60	--	
t_f	Fall Time		--	20	--	
Q_g	Total Gate Charge	$V_{DD}=20V, I_D=80A$	--	50	--	nC
Q_{gs}	Gate to Source Charge		--	18	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	21	--	

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Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	200	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S=100A, V_{GS}=0V$	--	--	1.2	V

Symbol	Parameter	Typ.	Units
$R_{θJC}$	Junction-to-Case ^{a2}	1.1	°C/W

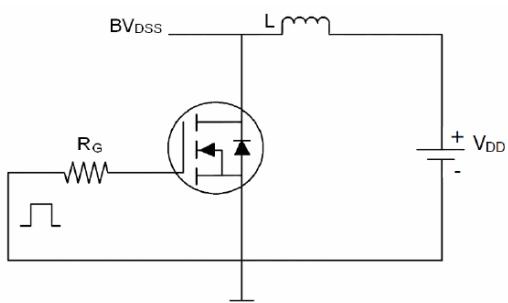
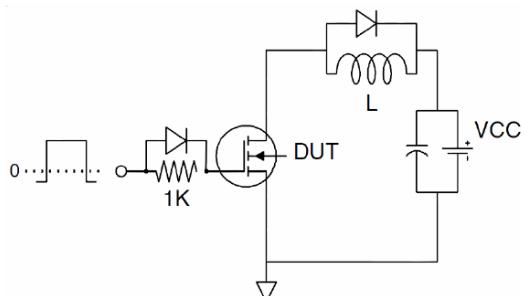
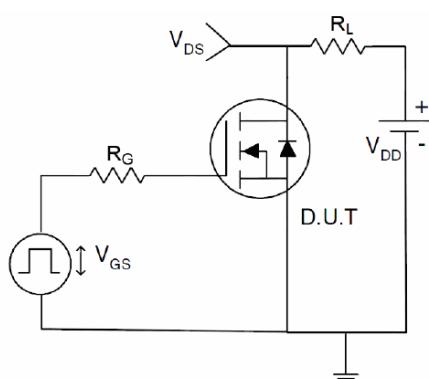
^{a1} : Repetitive Rating: Pulse width limited by maximum junction temperature.

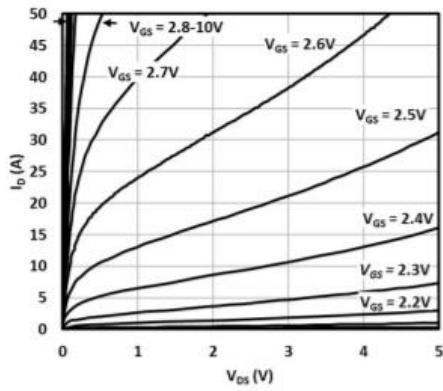
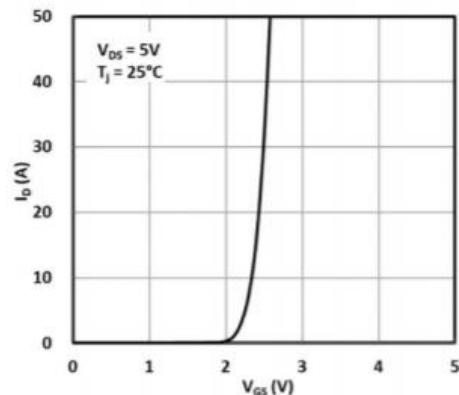
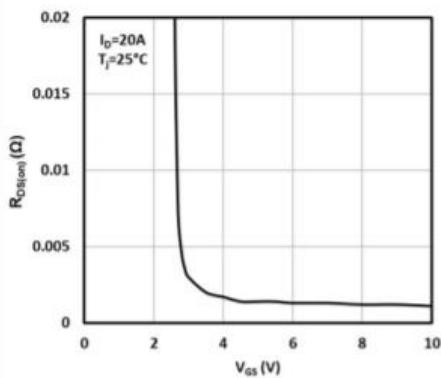
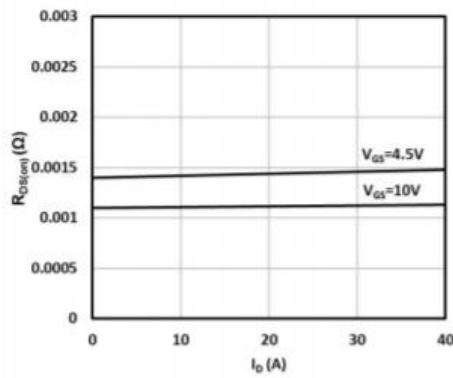
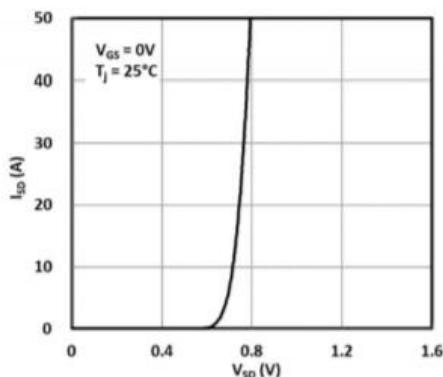
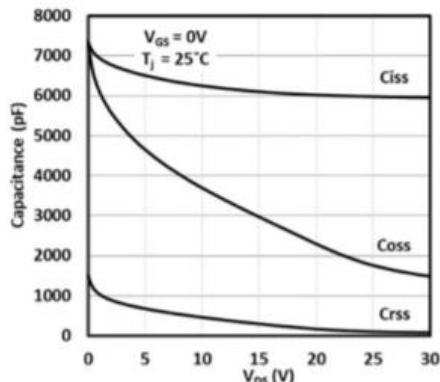
^{a2} : Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

^{a3} : Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

^{a4} : Guaranteed by design, not subject to production

^{a5} : EAS condition : $T_j=25^\circ\text{C}, V_{DD}=20\text{V}, V_G=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Test circuit
1) EAS test Circuit

2) Gate charge test Circuit

3) Switch Time Test Circuit


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Characteristics Curve :

Fig. 1 Output characteristics

Fig. 2 Transfer characteristics

Fig.3 On-resistance vs. gate voltage

Fig.4 On-resistance vs. drain current

Fig.5 Source-to-drain diode forward characteristics

Fig.6 Capacitance vs. drain-to-source voltage

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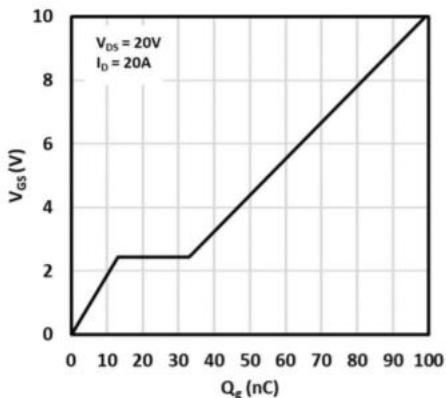


Fig.7 Gate-to-source voltage vs. gate charge

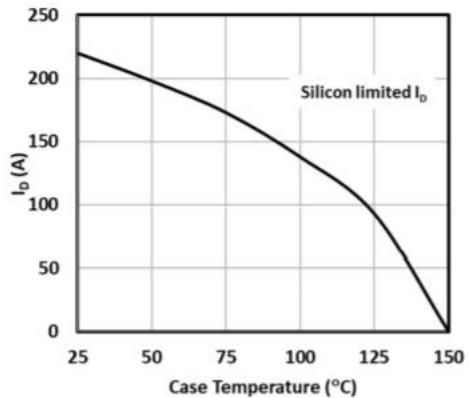


Fig.8 Maximum drain current vs. case temperature

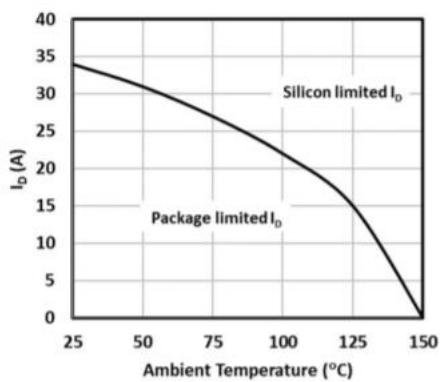


Fig. 9 Maximum drain current vs. ambient temperature

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