

General Description

The GL10NP06V-D8 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOP-8, which accords with the RoHS standard.

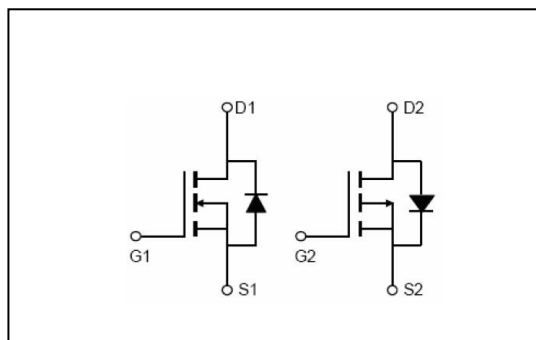
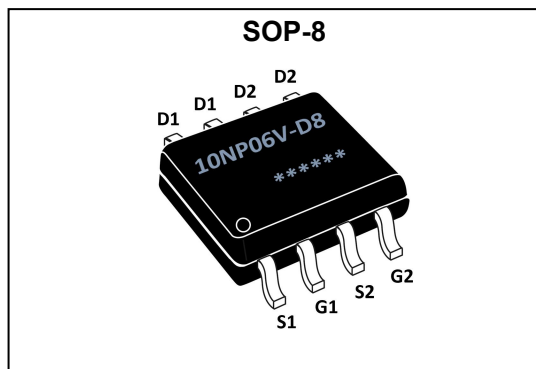
Features

● General Features N channel

- $V_{DS}=60V, I_D=10A$
- $R_{DS(ON)} < 18m\Omega @ V_{GS}=10V$ TYP. 15mΩ
- $R_{DS(ON)} < 25m\Omega @ V_{GS}=4.5V$ TYP. 18mΩ

● General Features P channel

- $V_{DS}=-60V, I_D=-10A$
- $R_{DS(ON)} < 75m\Omega @ V_{GS}=-10V$ TYP. 60.0mΩ
- $R_{DS(ON)} < 100m\Omega @ V_{GS}=-4.5V$ TYP. 70.0mΩ



Application

- H-bridge
- Inverters

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	$T_C=25^\circ C$	I_D	10	-10	A
	$T_C=100^\circ C$		7	-7	
Pulsed Drain Current (Note 1)		I_{DM}	40	-40	A
Maximum Power Dissipation	$T_C=25^\circ C$	P_D	2		W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 175		°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	75	°C/W
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GL10NP06V-D8

GL Silicon N+P Channel Power MOSFET

N-Channel Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.0	-	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	15	18	mΩ
		V _{GS} =4.5V, I _D =6A	-	18	25	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =10A	8	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{Iss}	V _{DS} =30V,V _{GS} =0V, F=1.0MHz	-	850	-	PF
Output Capacitance	C _{Oss}		-	95	-	PF
Reverse Transfer Capacitance	C _{rss}		-	51	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V ,R _L =2.5Ω V _{GS} =10V,R _G =3Ω	-	6.6	-	nS
Turn-on Rise Time	t _r		-	5.8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	32	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =6A, V _{GS} =10V	-	18		nC
Gate-Source Charge	Q _{gs}		-	4.8		nC
Gate-Drain Charge	Q _{gd}		-	6.8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =106A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	6	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =10A di/dt =100A/μs ^(Note3)	-	58	-	nS
Reverse Recovery Charge	Q _{rr}		-	60	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



GL10NP06V-D8

GL Silicon N+P Channel Power MOSFET

P-Channel Electrical Characteristics (TC=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D = -250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D = -250μA	-1.0	-	-3.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D = -10A	-	60	75	mΩ
		V _{GS} = -4.5V, I _D = -6A	-	70	100	mΩ
Forward Transconductance	g _{FS}	V _{DS} = -5V,I _D = -10A	6	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{Iss}	V _{DS} = -30V,V _{GS} =0V, F= 1.0MHz	-	960	-	PF
Output Capacitance	C _{Oss}		-	86	-	PF
Reverse Transfer Capacitance	C _{rss}		-	38	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} = -30V ,R _L =2.5Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}	V _{GS} = -10V,R _G =3Ω	-	25	-	nS
Turn-Off Fall Time	t _f		-	11	-	nS
Total Gate Charge	Q _g	V _{DS} = -30V,I _D = -6A, V _{GS} =10V	-	15.8		nC
Gate-Source Charge	Q _{gs}		-	3		nC
Gate-Drain Charge	Q _{gd}		-	3.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S = -10A	-		-1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-6	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = -10A di/dt = 100A/μs ^(Note3)	-	58	-	nS
Reverse Recovery Charge	Q _{rr}		-	60	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

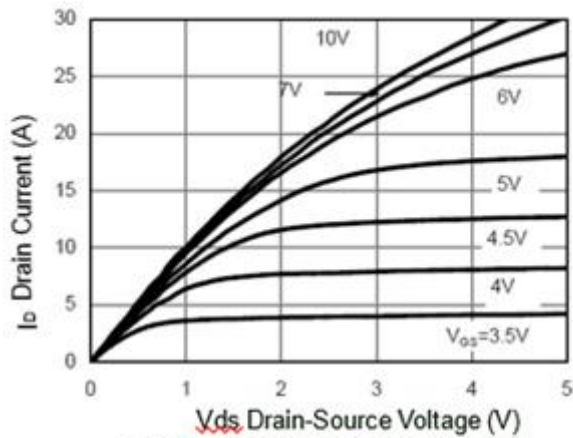


Figure 1 Output Characteristics

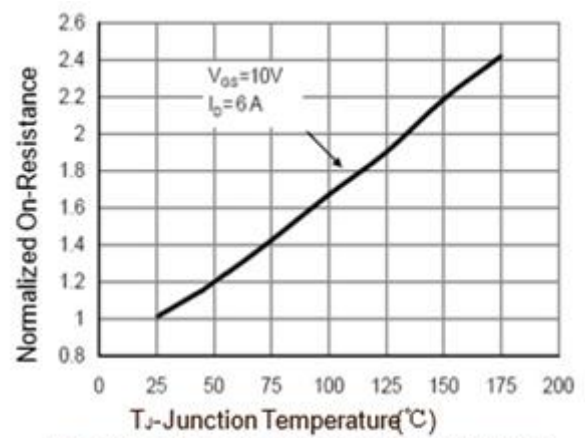


Figure 4 $R_{ds(on)}$ -Junction Temperature

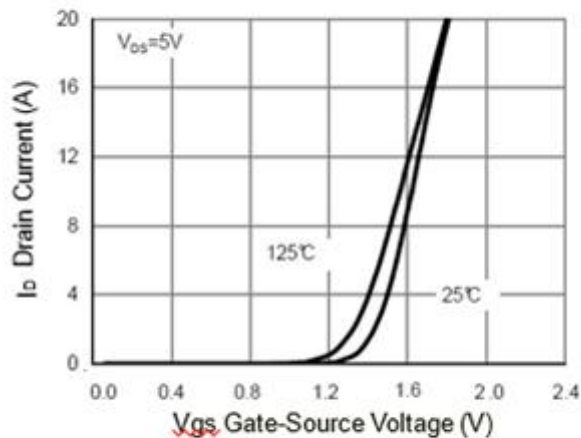


Figure 2 Transfer Characteristics

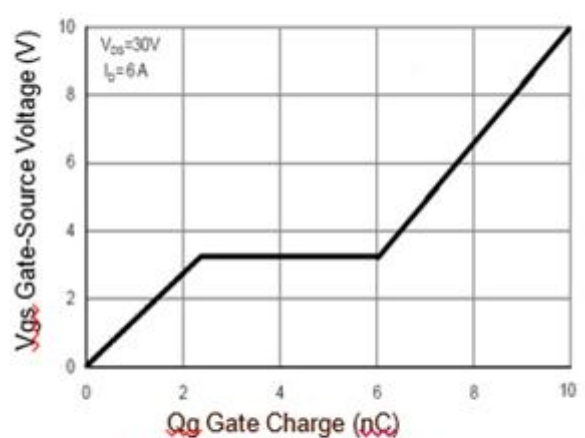


Figure 5 Gate Charge

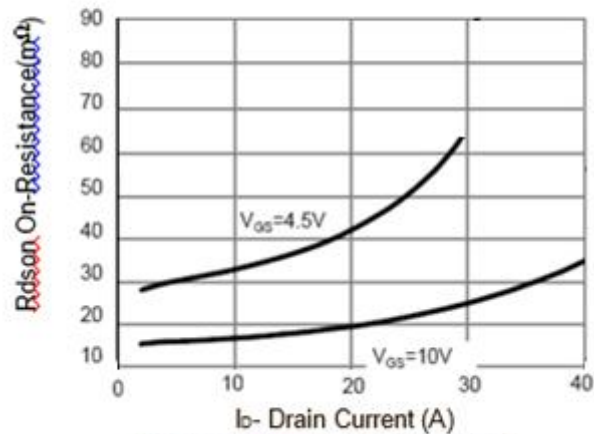


Figure 3 $R_{ds(on)}$ -Drain Current

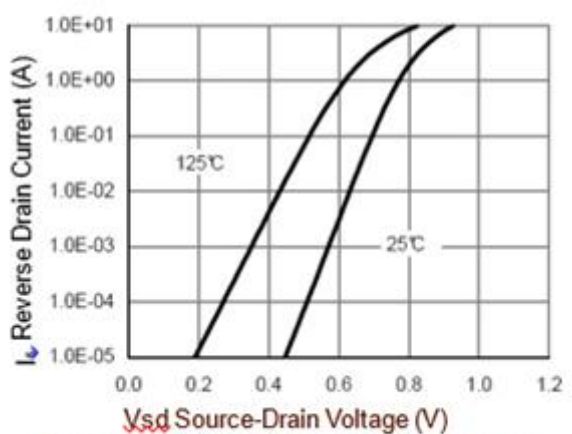


Figure 6 Source- Drain Diode Forward

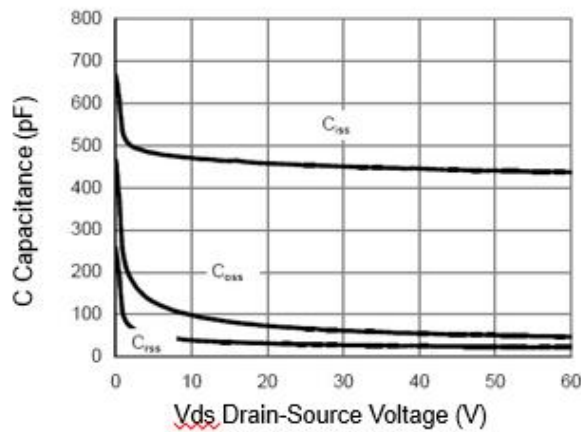


Figure 7 Capacitance vs V_{ds}

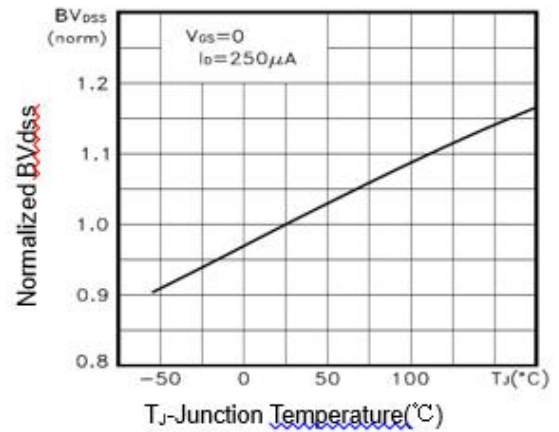


Figure 9 BV_{dss} vs Junction Temperature

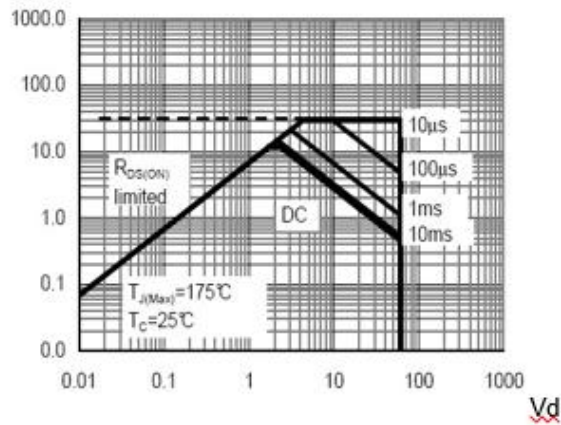


Figure 8 Safe Operation Area

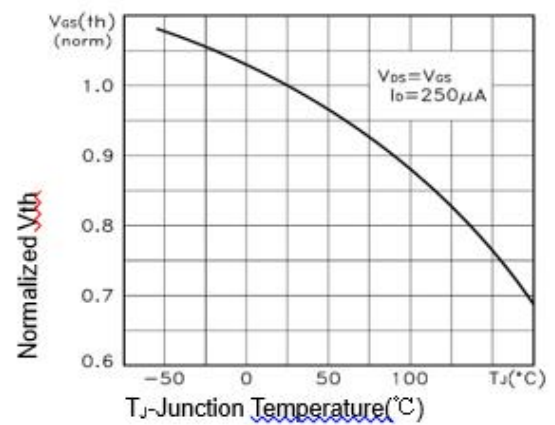
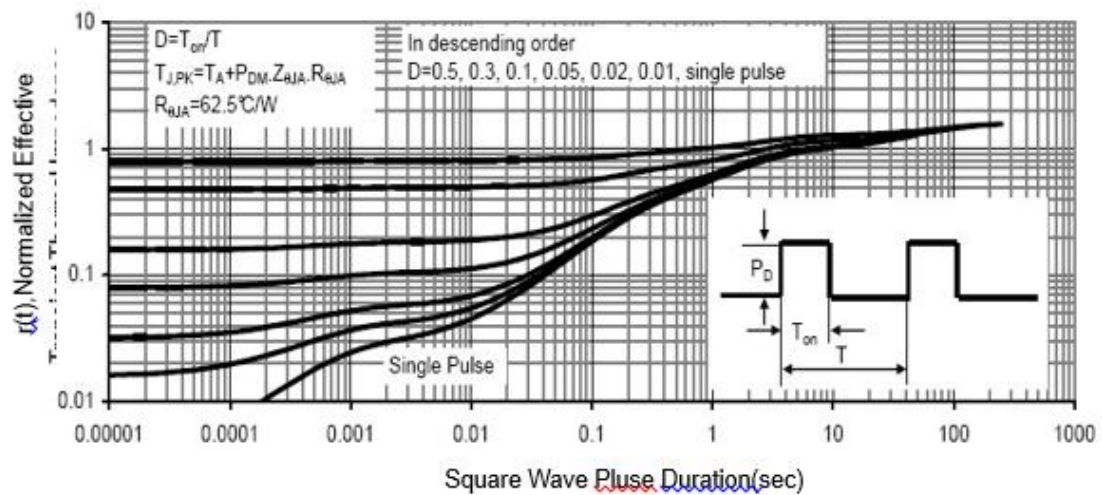


Figure 10 $V_{gs(th)}$ vs Junction Temperature



P-Channel Typical Electrical and Thermal Characteristics (Curves)

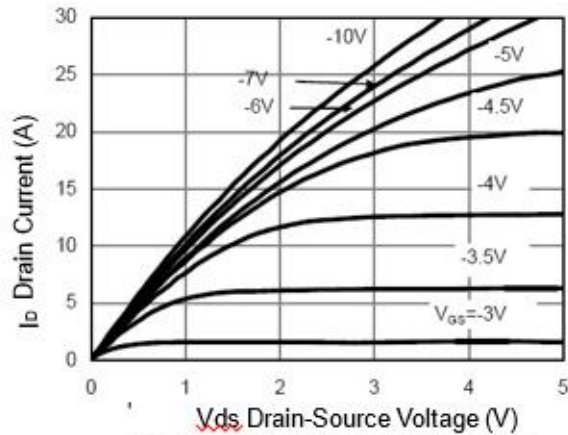


Figure 1 Output Characteristics

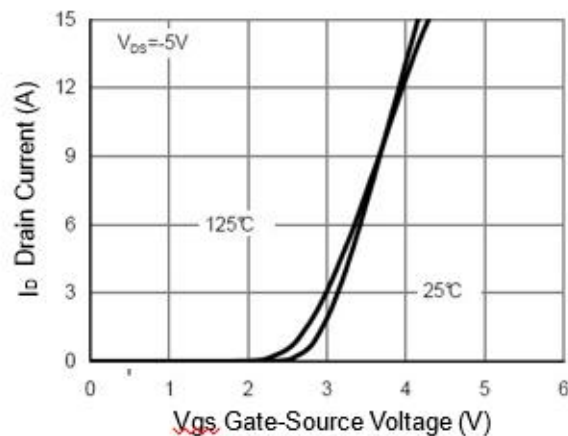


Figure 2 Transfer Characteristics

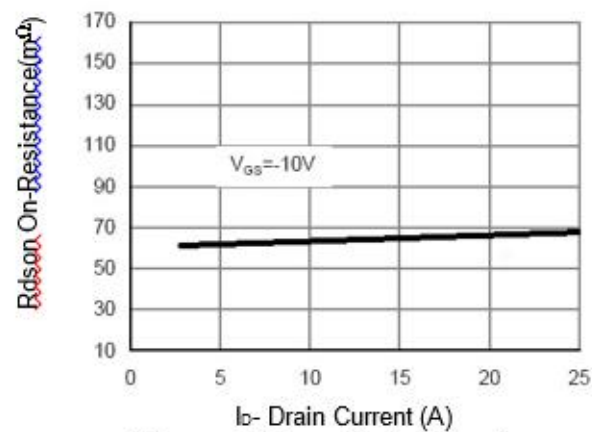


Figure 3 $R_{DS(on)}$ -Drain Current

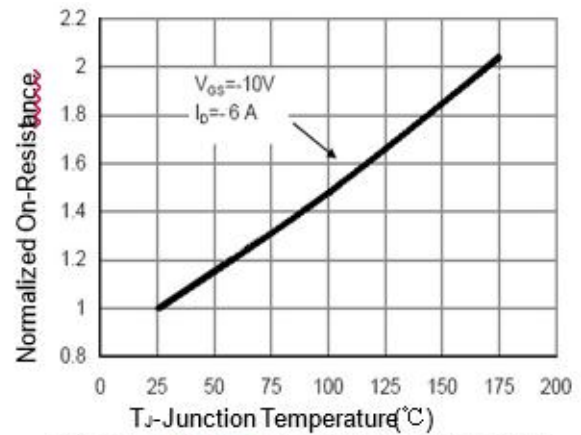


Figure 4 $R_{DS(on)}$ -Junction Temperature

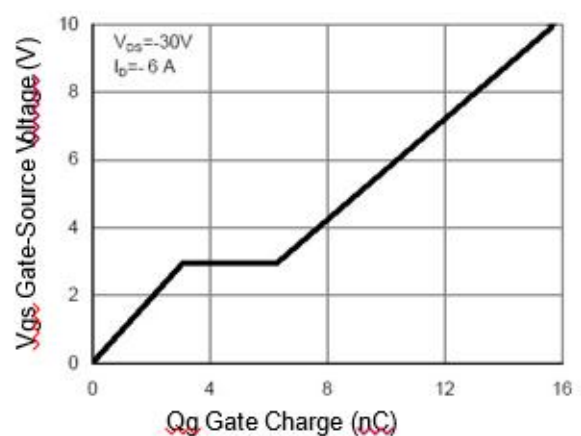


Figure 5 Gate Charge

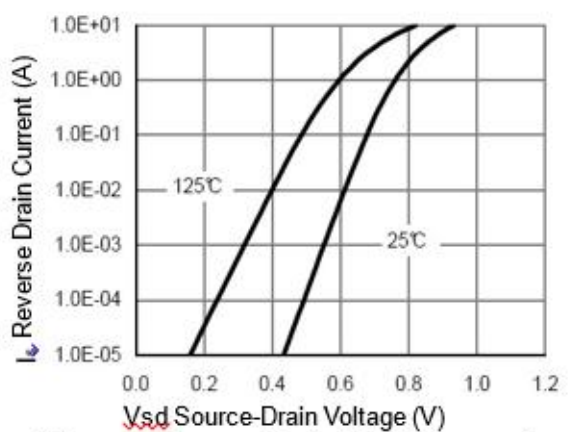


Figure 6 Source-Drain Diode Forward

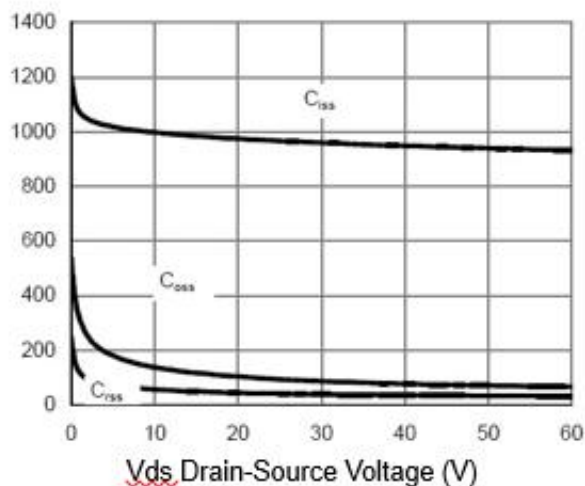


Figure 7 Capacitance vs V_{ds}

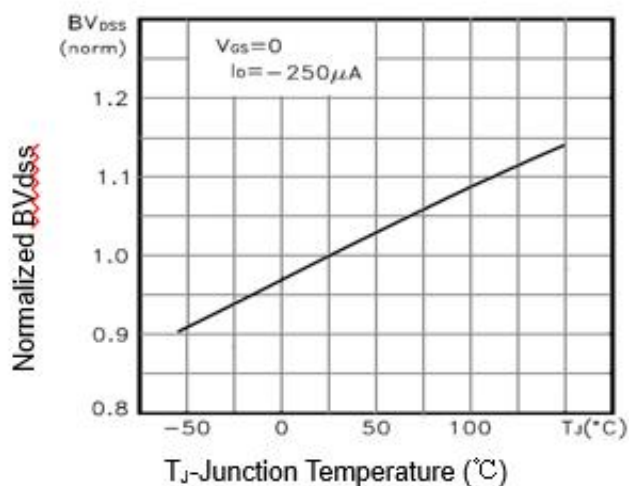


Figure 9 BV_{dss} vs Junction Temperature

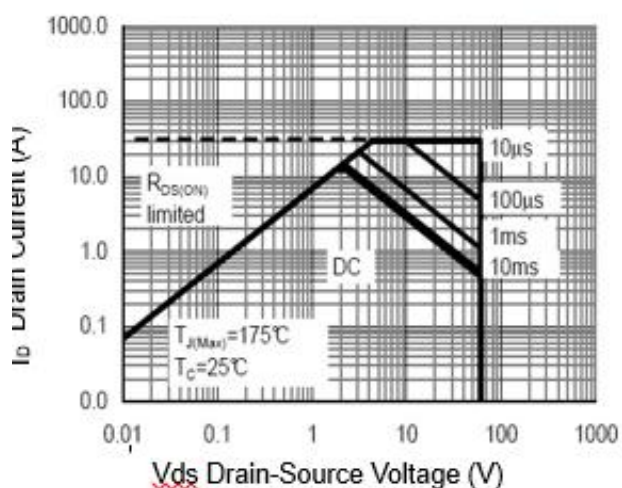


Figure 8 Safe Operation Area

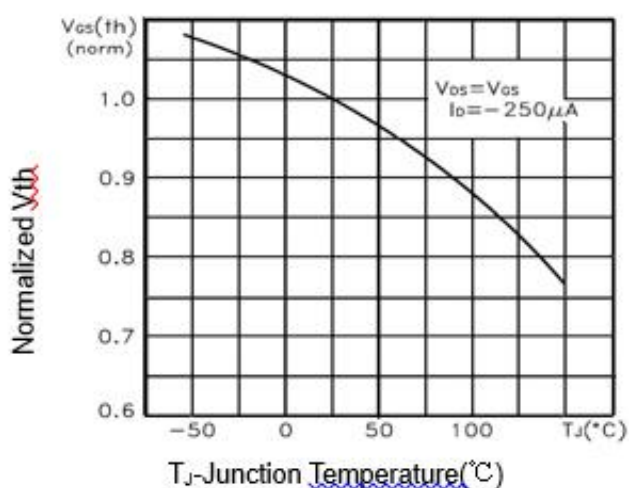


Figure 10 $V_{gs(th)}$ vs Junction Temperature

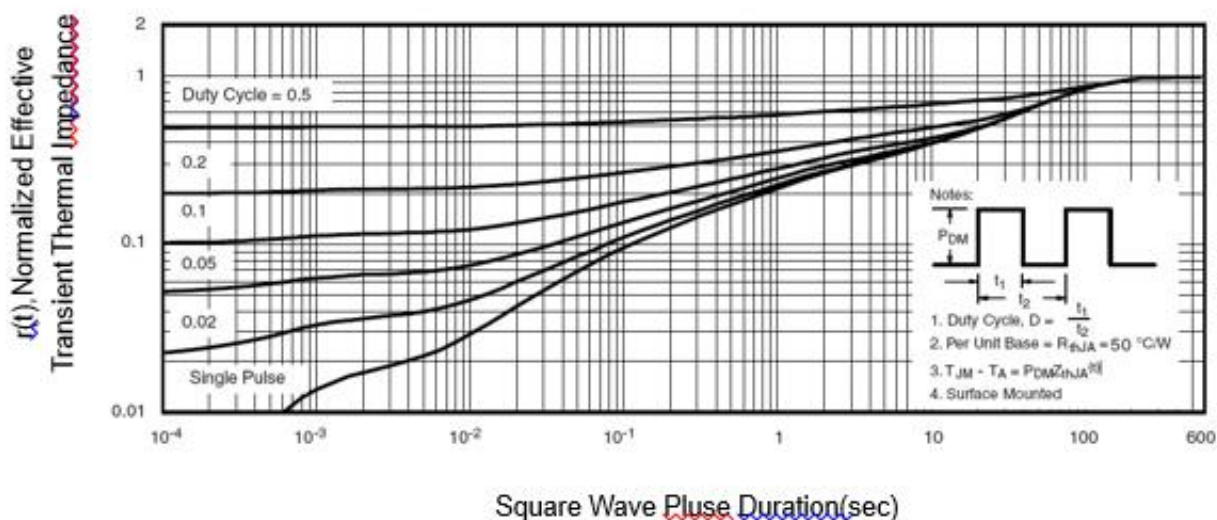


Figure 11 Normalized Maximum Transient Thermal Impedance