GL01N60

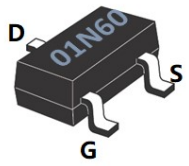
Silicon N-Channel Power MOSFET

V_{DSS}	600	V
I_D	50	mA
$P_D(T_C=25℃)$	1.39	W
$R_{DS(ON).TYP.}$	120	Ω

General Description

GL1N60, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is SOT-23, which accords with the RoHS standard.

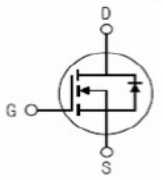
SOT-23



Features

- Fast Switching
- Low ON Resistance
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications

- Power switch circuit of adaptor and charger

Absolute (Tc=25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	50	mA
	Continuous Drain Current T_C=100 °C	35	mA
I_{DM}[a1]	Pulsed Drain Current	200	mA
V_{GS}	Gate-to-Source Voltage	±20	V
dv/dt[a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	1.39	W
	Derating Factor above 25°C	0.89	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	90	℃/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	℃/ W

Electrical Characteristics (Tc= 25℃ unless otherwise specified)

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	I_D=250uA,Reference25℃	--	0.55	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS}=600V, V_{GS}=0V,T_a=25℃	--	--	1.0	μA
		V_{DS}=480V, V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=25mA	--	120	160	Ω
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=4.5V,I_D=20mA	--	130	180	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	0.6	--	2.0	V
g_{fs}	Forward Trans conductance	V_{DS}=15V,I_D=20mA	--	0.15	--	S

Pulse width＜380μs; duty cycle＜2%.

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	8.8	--	pF
C_{oss}	Output Capacitance		--	1.5	--	
C_{rss}	Reverse Transfer Capacitance		--	0.6	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=20mA,V_{DD}=300V V_{GS}=10V,R_g=25Ω	--	3.5	--	ns
t_r	Rise Time		--	4.0	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	10	--	
t_f	Fall Time		--	15	--	
Q_g	Total Gate Charge	I_D=20mA,V_{DD}=300V V_{GS}=10V	--	0.8	--	nC
Q_{gs}	Gate to Source Charge		--	0.09	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	0.4	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	50	mA
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	200	mA
V_{SD}	Diode Forward Voltage	I_S=50mA,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=20mA,T_j=25℃	--	90	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/μs,V_{GS}=0V	--	8	--	μC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: L=0.1mH, I_D=50mA, Start T_J=25℃

a3: I_{SD}=50mA,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curves

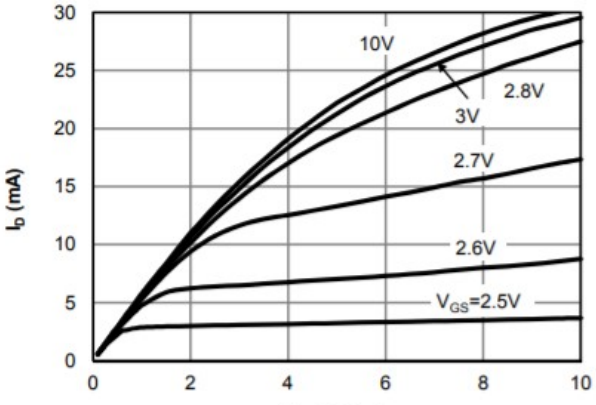


Figure 1: On-Region Characteristics

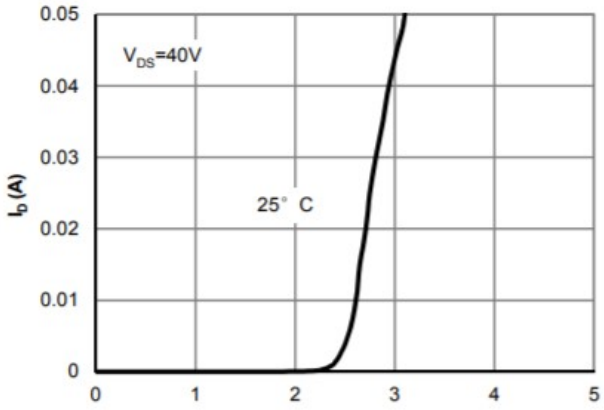


Figure 2: Transfer Characteristics

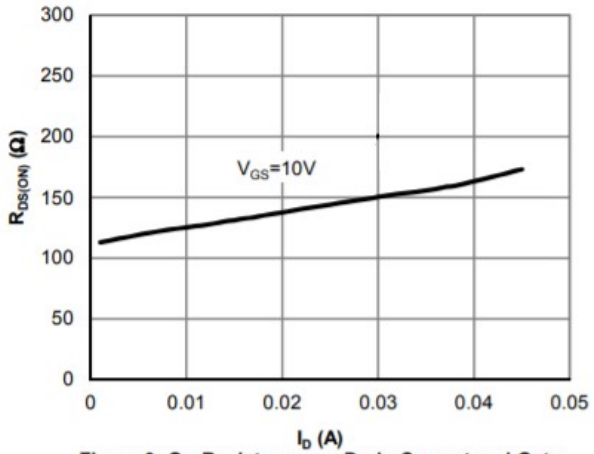


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

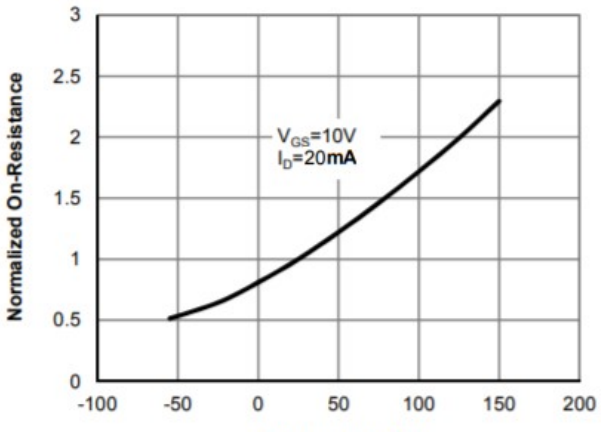


Figure 4: On-Resistance vs. Junction Temperature

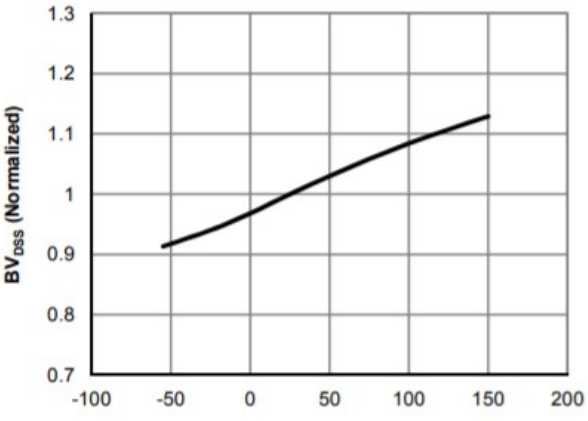


Figure 5: Break Down vs. Junction Temperature

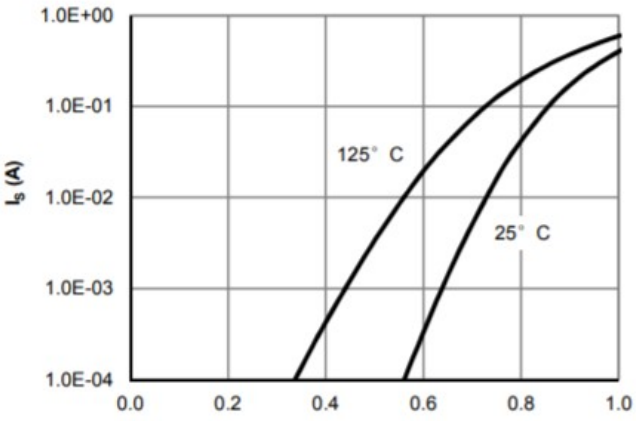


Figure 6: Body-Diode Characteristics

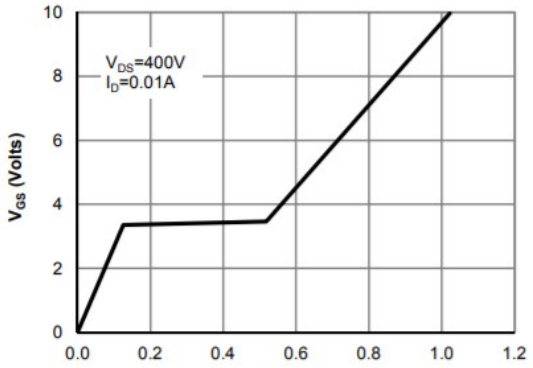


Figure 7: Gate-Charge Characteristics

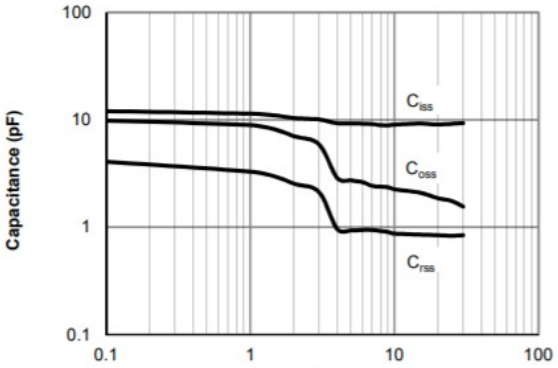


Figure 8: Capacitance Characteristics

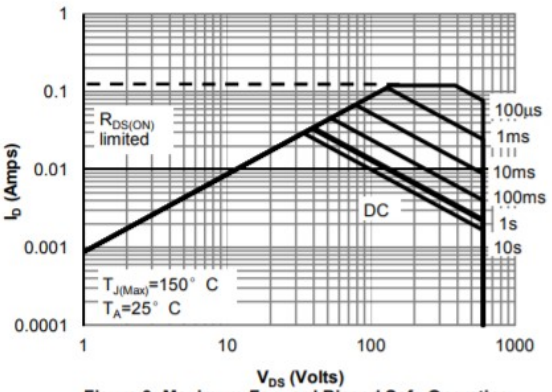


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

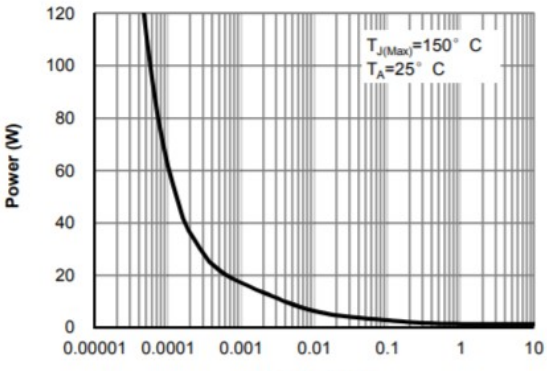


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

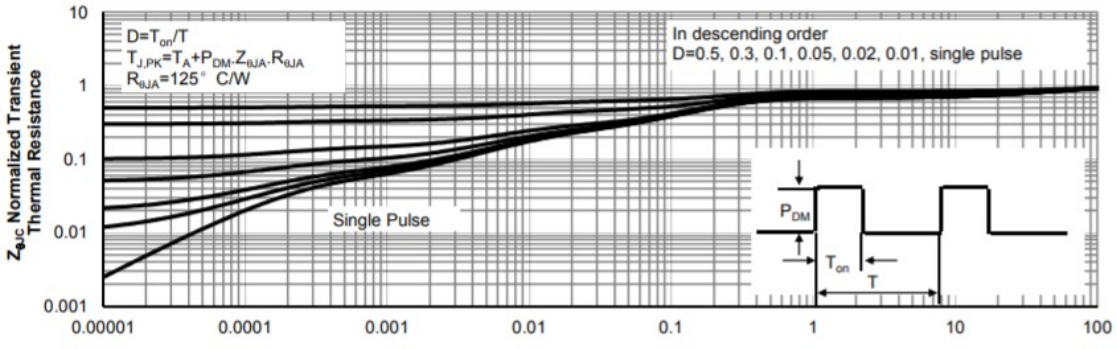


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)