GL40N50AN

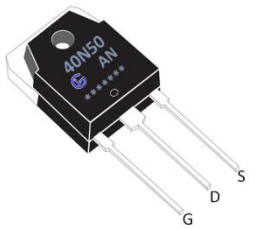
Silicon N-Channel Power MOSFET

V_{DSS}(T_C=150℃)	500	V
I_D	40	A
P_D(T_C=25℃)	250	W
$R_{DS(ON)}$	79	mΩ

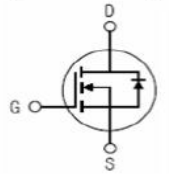
General Description

GL40N50AN, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3P(N), which accords with the RoHS standard.

TO-3P(N)



Inner Equivalent Principium Chart



Features

- Fast Switching
- ESD Improved Capability
- Low Gate Charge (Typical Data: 140nC)
- Low Reverse transfer capacitances(Typical: 80pF)
- 100% Single Pulse avalanche energy Test

Applications

- Power switch circuit of PC POWER

Absolute (Tc=25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	40	A
	Continuous Drain Current T_C=100 °C	28	A
I_{DM} [a1]	Pulsed Drain Current	160	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy	3500	mJ
E_{Ar} [a1]	Avalanche Energy ,Repetitive	400	mJ
I_{AR} [a1]	Avalanche Current	8.9	A
dv/dt [a2]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	250	W
	Derating Factor above 25°C	2	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	℃/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	℃/ W

Electrical Characteristics (Tc= 25℃ unless otherwise specified)

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	500	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=500V, V_{GS}=0V,T_a=25℃	--	--	1.0	μA
		V_{DS}=400V, V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	79	90	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	V_{DS}=30V,I_D=20A	--	21	--	S
Pulse width<380μs; duty cycle<2%.						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	8260	--	pF
C_{oss}	Output Capacitance		--	730	--	
C_{rss}	Reverse Transfer Capacitance		--	80	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=40A,V_{DD}=250V V_{GS}=10V,R_g=25Ω	--	69	--	ns
t_r	Rise Time		--	125	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	488	--	
t_f	Fall Time		--	150	--	
Q_g	Total Gate Charge	I_D=40A,V_{DD}=250V V_{GS}=10V	--	145	--	nC
Q_{gs}	Gate to Source Charge		--	23	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	49	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	40	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	160	A
V_{SD}	Diode Forward Voltage	I_S=40A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=40A,T_j=25℃	--	490	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/μs,V_{GS}=0V	--	4.82	--	uC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: I_{SD}=40A,di/dt≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curves

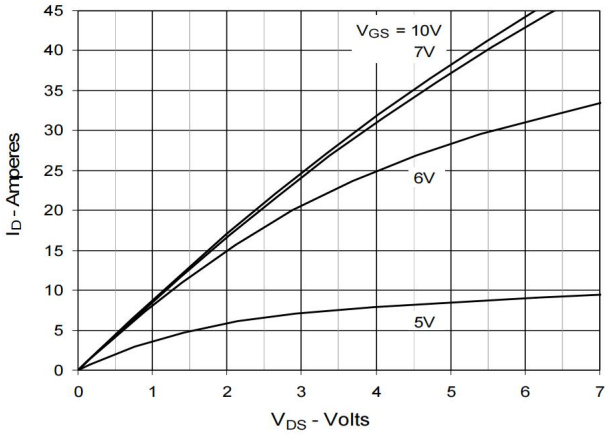


Fig. 1. Output Characteristics

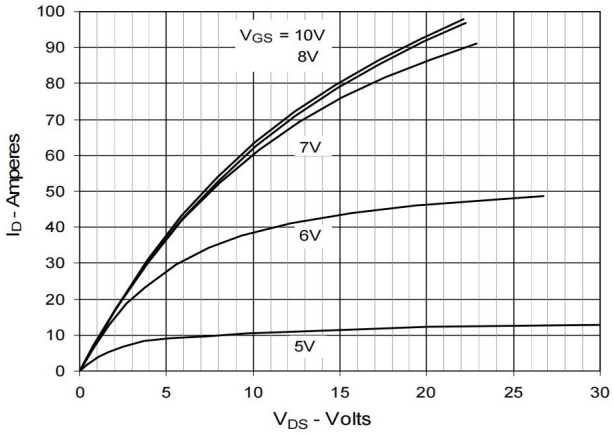


Fig. 2. Extended Output Characteristics

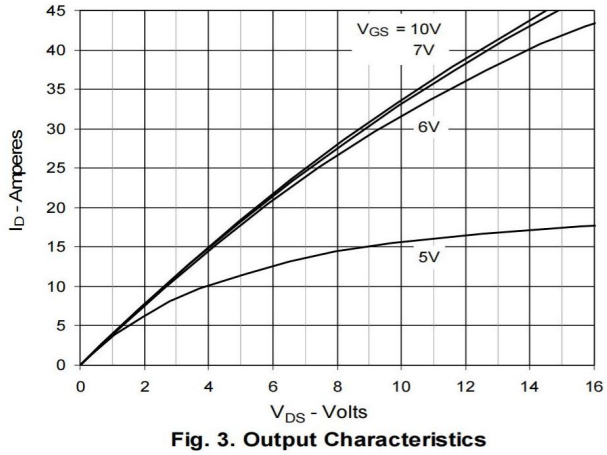


Fig. 3. Output Characteristics

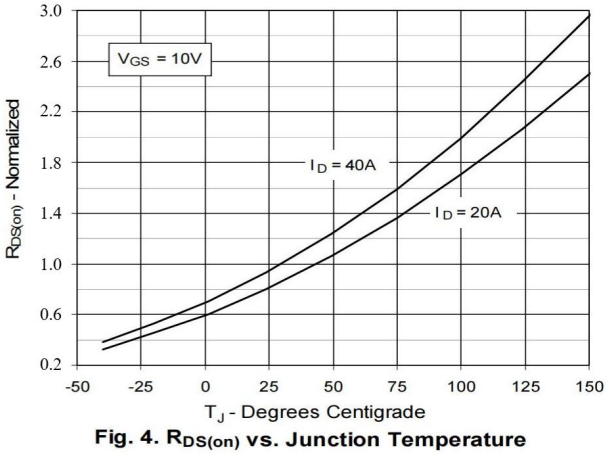


Fig. 4. $R_{DS(on)}$ vs. Junction Temperature

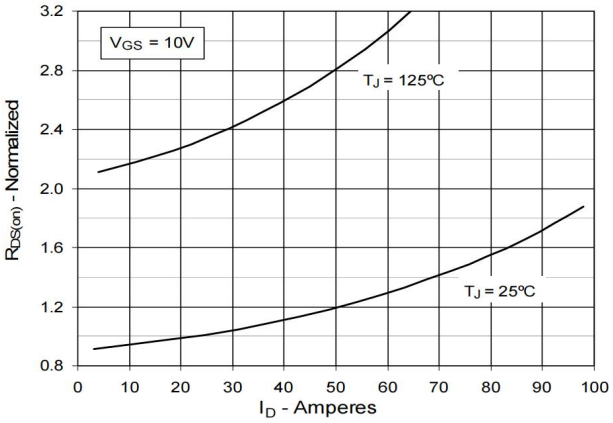


Fig. 5. $R_{DS(on)}$ vs. Drain Current

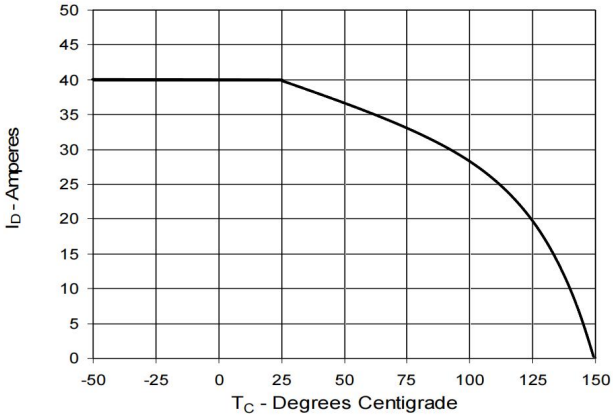


Fig. 6. Maximum Drain Current vs. Case Temperature

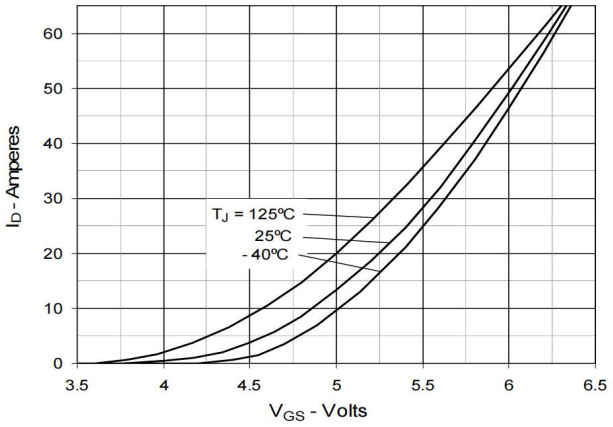


Fig. 7. Input Admittance

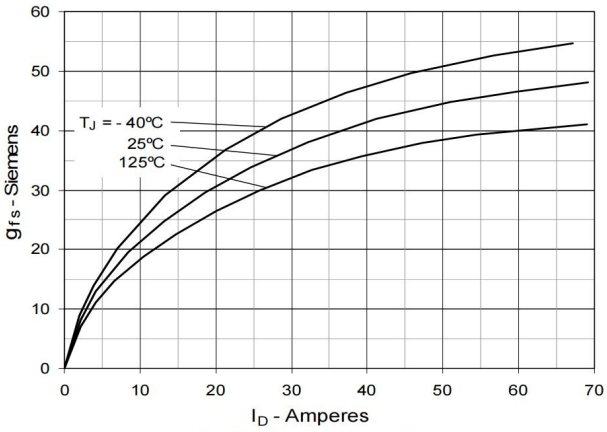


Fig. 8. Transconductance

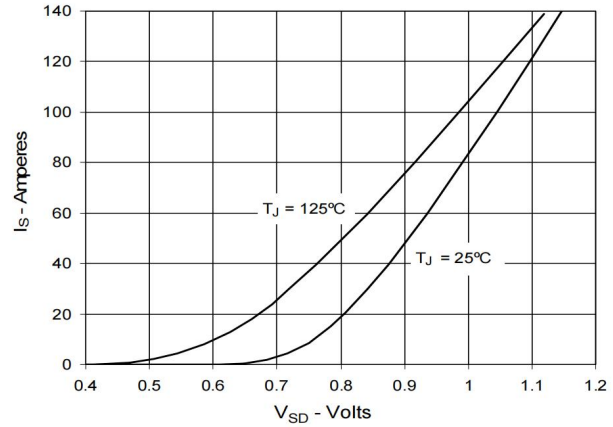


Fig. 9. Forward Voltage Drop of Intrinsic Diode

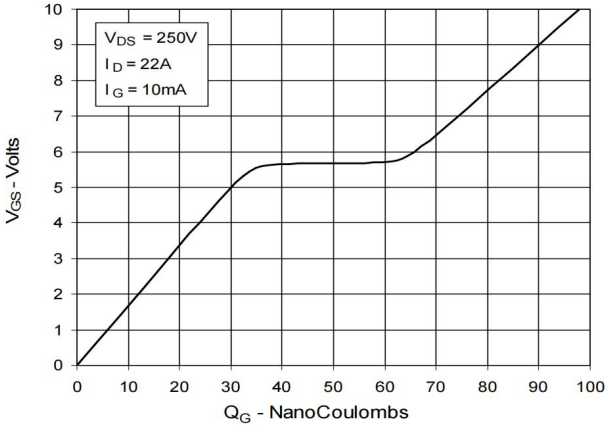


Fig. 10. Gate Charge

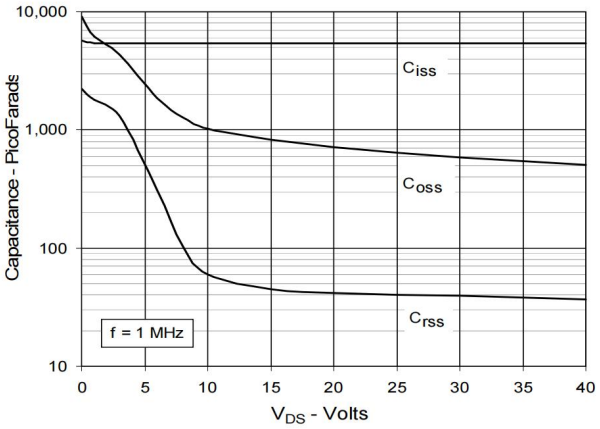


Fig. 11. Capacitance

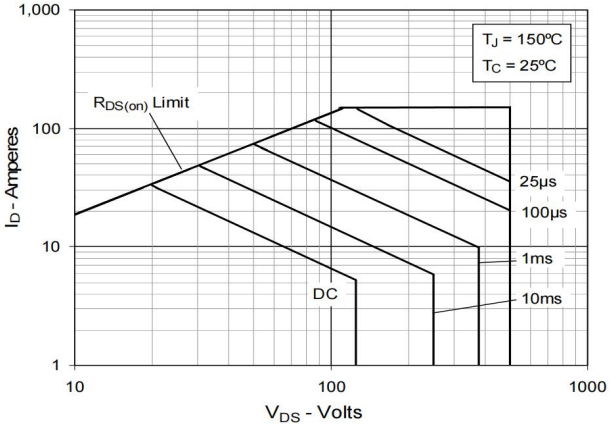


Fig. 12. Forward-Bias Safe Operating Area

Fig. 13. Maximum Transient Thermal Resistance