

General Description:

GL74N20A47, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

Features:

- Fast Switching
- ESD Improved Capability
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications:

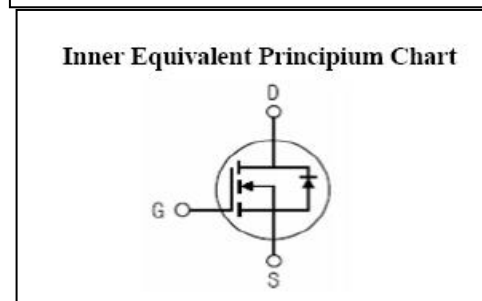
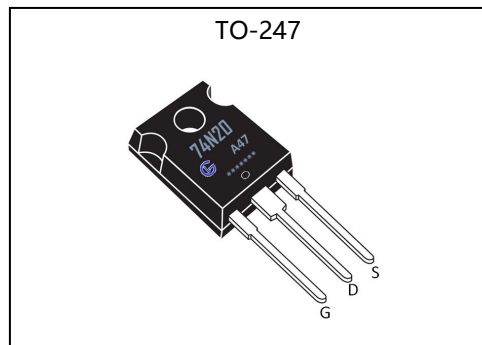
- Power switch circuit of POWER

Absolute (T_c=25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	200	V
I _D	Continuous Drain Current	74	A
	Continuous Drain Current T _C =100 °C	52	A
I _{DM} ^{a1}	Pulsed Drain Current(pulse width limited by T _{JM})	225	A
V _{GS}	Gate-to-Source Voltage	± 30	V
E _{AS}	Single Pulse Avalanche Energy	2800	mJ
E _{Ar} ^{a1}	Avalanche Energy ,Repetitive	220	mJ
I _{AR} ^{a1}	Avalanche Current	74	A
dv/dt ^{a2}	Peak Diode Recovery dv/dt	5.0	V/ns
P _D	Power Dissipation	360	W
	Derating Factor above 25°C	2.88	W/°C
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

V _{DSS} (T _C =150°C)	200	V
I _D	74	A
P _D (T _C =25°C)	360	W
R _{DS(ON)TYPE}	27	mΩ





GL74N20A47

Silicon N-Channel Power MOSFET

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.347	°C/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	°C/ W

Electrical Characteristics (T_c= 25°C unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	200	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=200V, V_{GS}=0V, T_a=25^\circ C$	--	--	1.0	μA
		$V_{DS}=160V, V_{GS}=0V, T_a=125^\circ C$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=37A$	--	27	35	m Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=40A$	--	50	--	S
Pulse width<380 μs ; duty cycle<2%.						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	4500	--	pF
C_{oss}	Output Capacitance		--	400	--	
C_{rss}	Reverse Transfer Capacitance		--	100	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=37A, V_{DD}=100V$ $V_{GS}=10V, R_g=12\Omega$	--	36	--	ns
t_r	Rise Time		--	85	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	190	--	
t_f	Fall Time		--	92	--	
Q_g	Total Gate Charge	$I_D=40A, V_{DD}=100V$ $V_{GS}=10V$	--	83	--	nC
Q_{gs}	Gate to Source Charge		--	20	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	40	--	



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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	74	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	225	A
V_{SD}	Diode Forward Voltage	$I_S=72A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=72A, T_j=25^{\circ}C$	--	410	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/\mu s, V_{GS}=0V$	--	3.6	--	μC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $I_{SD}=74A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS},$ Start $T_j=25^{\circ}C$

Characteristics Curve:

Fig. 1. Output Characteristics @ 25°C

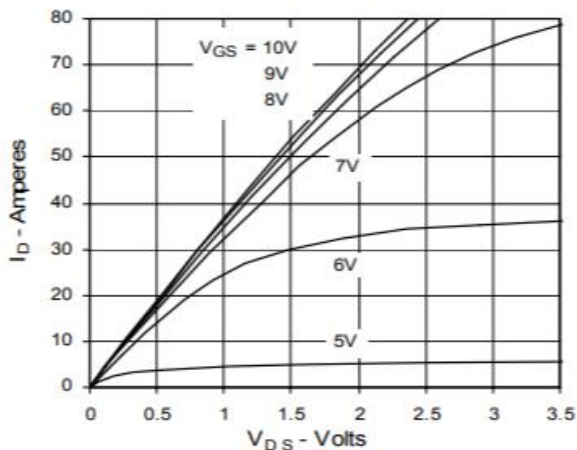


Fig. 2. Extended Output Characteristics @ 25°C

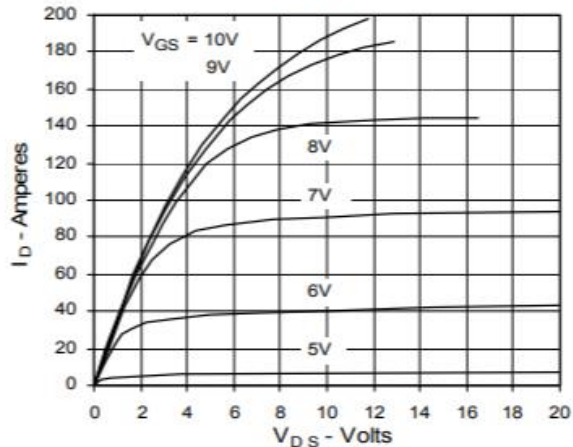


Fig. 3. Output Characteristics @ 150°C

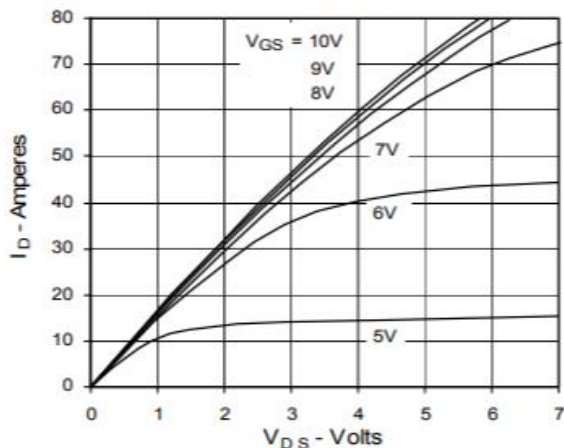


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

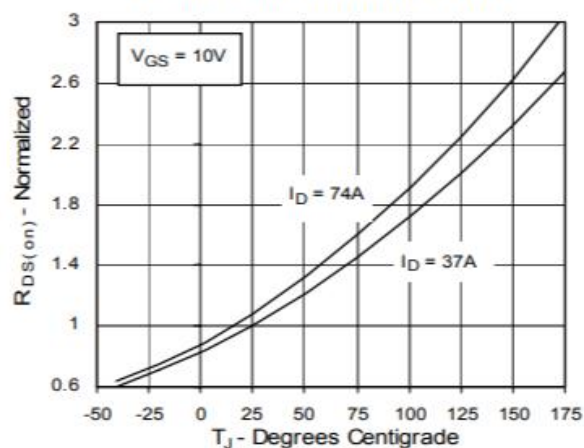


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

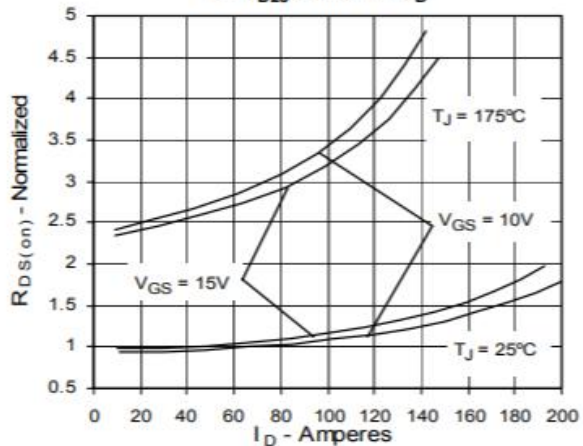
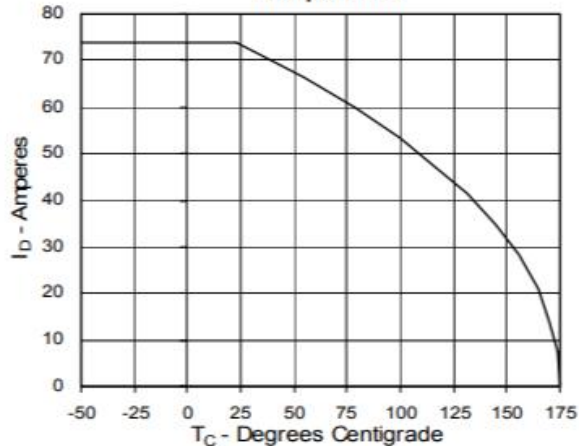


Fig. 6. Drain Current vs. Case Temperature





GL74N20A47

Silicon N-Channel Power MOSFET

Fig. 7. Input Admittance

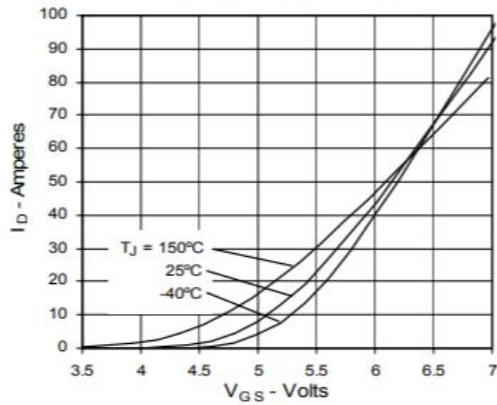


Fig. 8. Transconductance

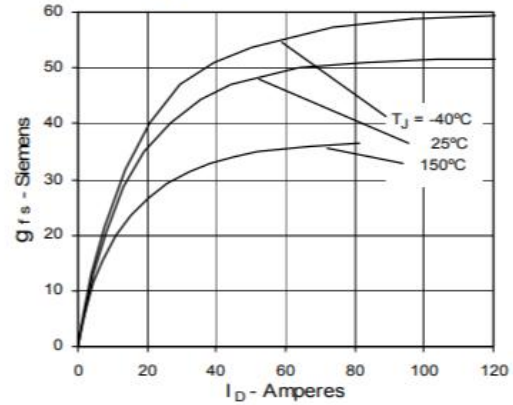


Fig. 9. Source Current vs. Source-To-Drain Voltage

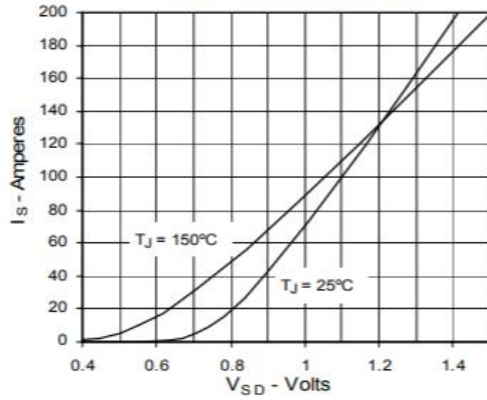


Fig. 10. Gate Charge

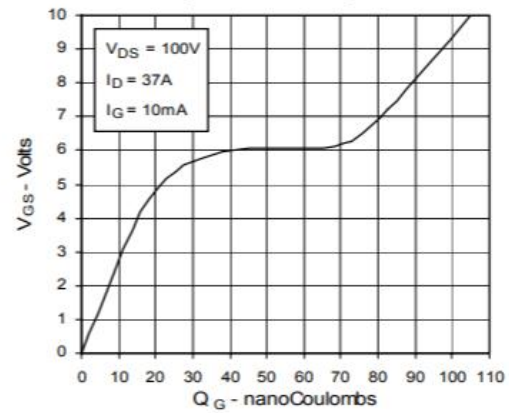


Fig. 11. Capacitance

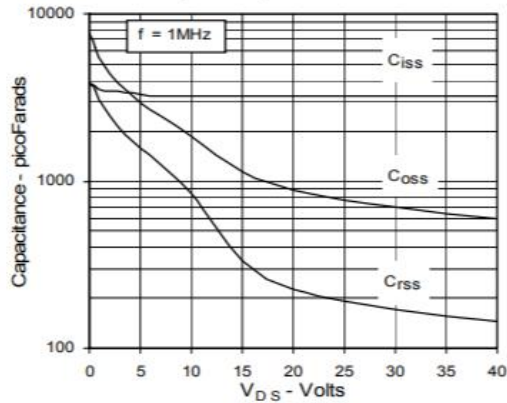
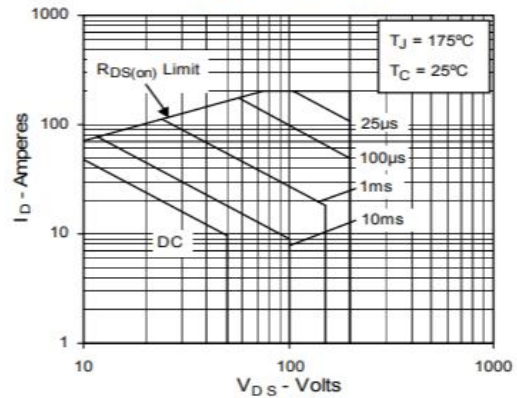


Fig. 12. Forward-Bias Safe Operating Area





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Fig. 13. Maximum Transient Thermal Resistance

