GL1502

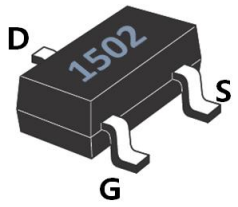
GL Silicon N-Channel Power MOSFET

General Description

The GL1502 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the RoHS standard.

V_{DSS}	150	V
I_D	2	A
P_D	1.5	W
$R_{DS(ON)MAX}$	2.2	Ω

SOT-23



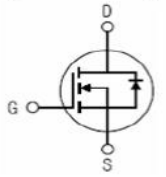
Features

- $R_{DS(ON)}$ <2.2Ω @ V_{GS}=10V)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Inner Equivalent Principium Chart



Absolute (Tc= 25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	150	V
I_D	Continuous Drain Current	2	A
I_{DM}	Pulsed Drain Current	6	A
V_{GS}	Gate-to-Source Voltage	±25	V
P_D	Power Dissipation	1.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃

Caution :Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

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Electrical Characteristics (Tc= 25℃ unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	150	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=150V, V_{GS}= 0V,T_a=25℃	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+25V	--	--	1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-25V	--	--	-1	μA

ON Characteristics[a3]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=1.0A	--	--	2.2	Ω
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=4.5V,I_D=1.0A	--	--	2.5	Ω
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=2.5V,I_D=0.5A	--	--	3.0	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	0.5	--	1.5	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V,I_D=1.5A	--	3	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=25V f=1.0MHz	--	235	--	pF
C_{oss}	Output Capacitance		--	36	--	
C_{rss}	Reverse Transfer Capacitance		--	20	--	

Resistive Switching Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=75V,I_D=1A, R_L=75Ω V_{GS}=10V,R_G=6Ω	--	8	--	ns
t_r	Rise Time		--	10	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	20	--	
t_f	Fall Time		--	15	--	
Q_g	Total Gate Charge	V_{DD}=75V, I_D=1.5A V_{GS}=10V	--	8	--	nC
Q_{gs}	Gate to Source Charge		--	1.4	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	2.1	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current [a2](Body Diode)		--	--	2	A
V_{SD}	Diode Forward Voltage[a3]	I_S=2A,V_{GS}=0V	--	--	1.2	V

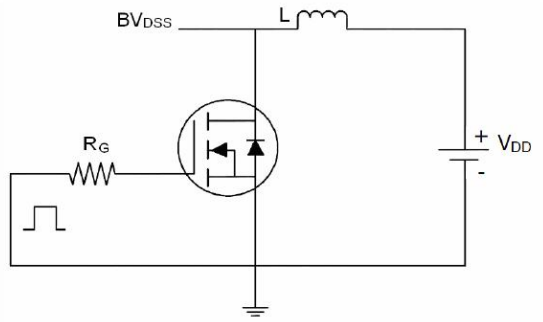
Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient[a2]	100	℃/W

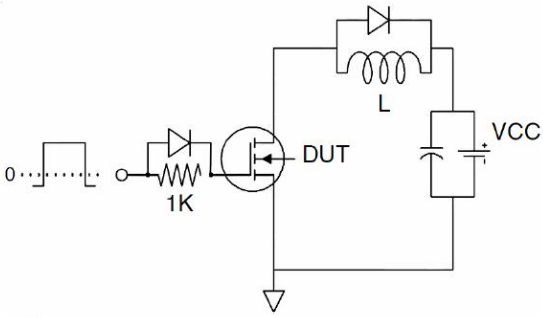
[a1]: Repetitive Rating: Pulse width limited by maximum junction temperature.
[a2]: Surface Mounted on FR4 Board, t≤10sec.
[a3]: Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.
[a4]: Guaranteed by design, not subject to production

Test Circuits

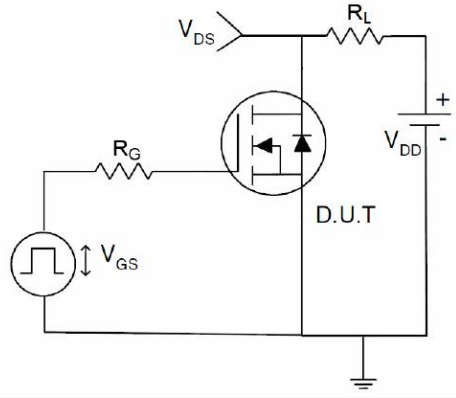
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Characteristics Curves

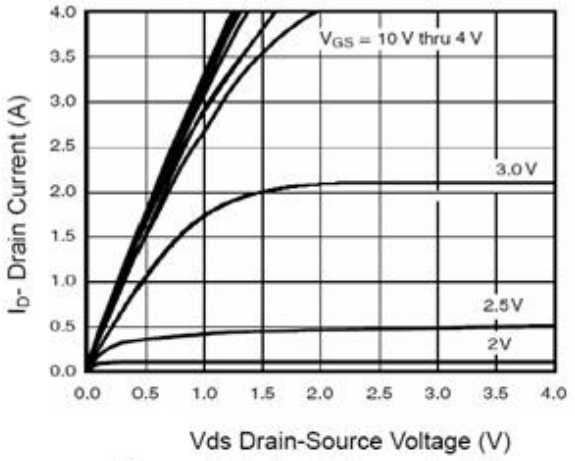


Figure 1 Output Characteristics

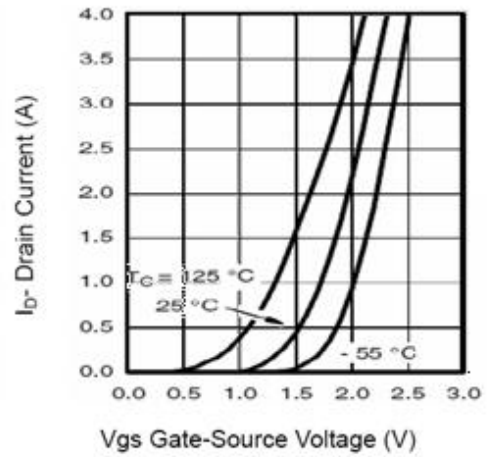


Figure 2 Transfer Characteristics

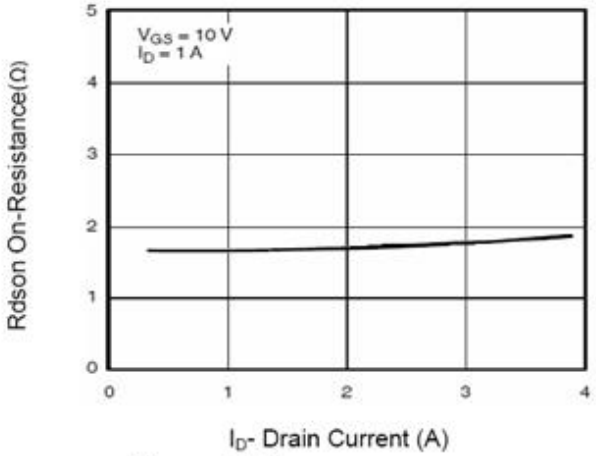


Figure 3 Rdson- Drain Current

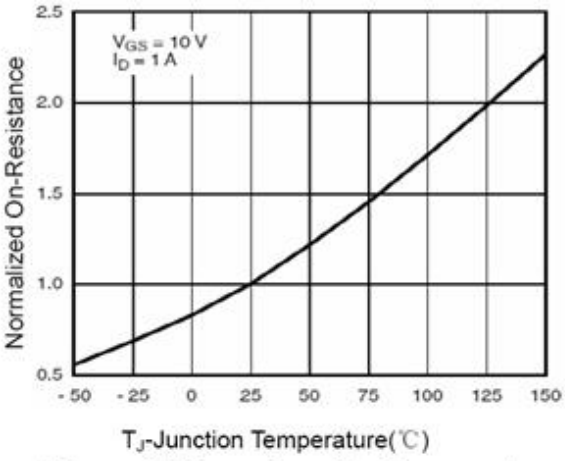


Figure 4 Rdson- Junction Temperature

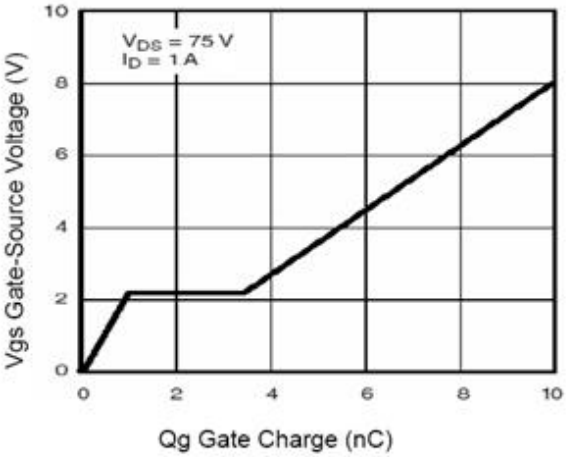


Figure 5 Gate Charge

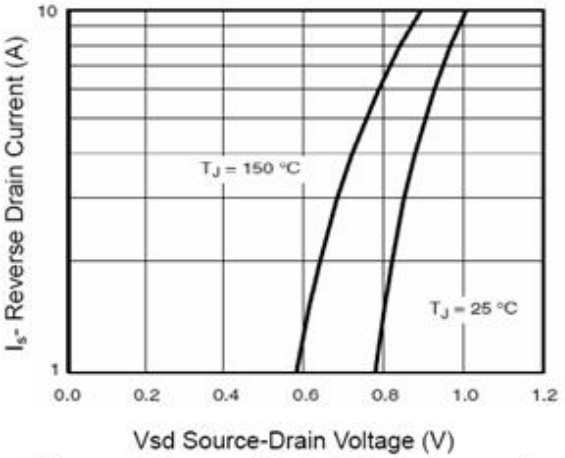


Figure 6 Source- Drain Diode Forward

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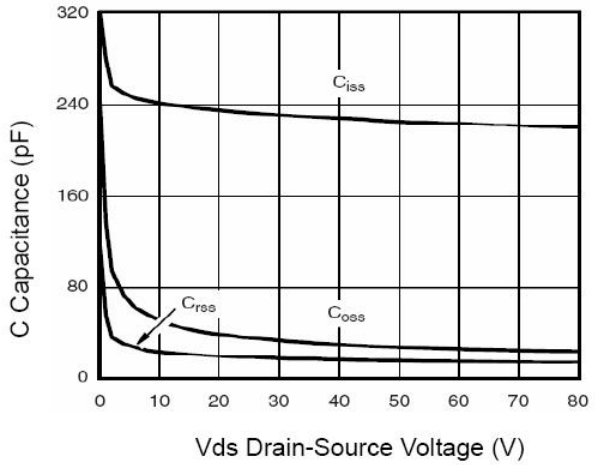

Figure 7 Capacitance vs Vds

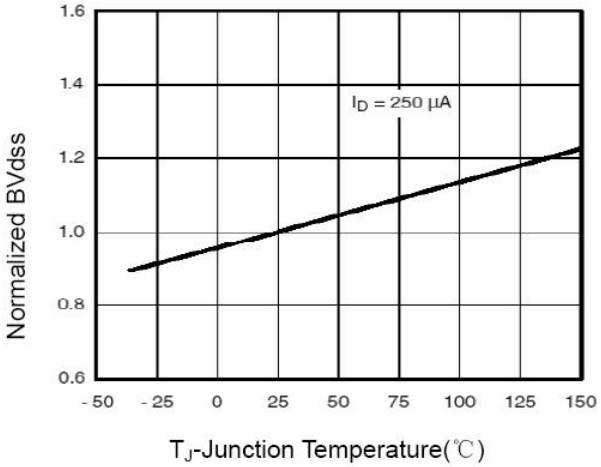

Figure 9 BV_{DSS} vs Junction Temperature

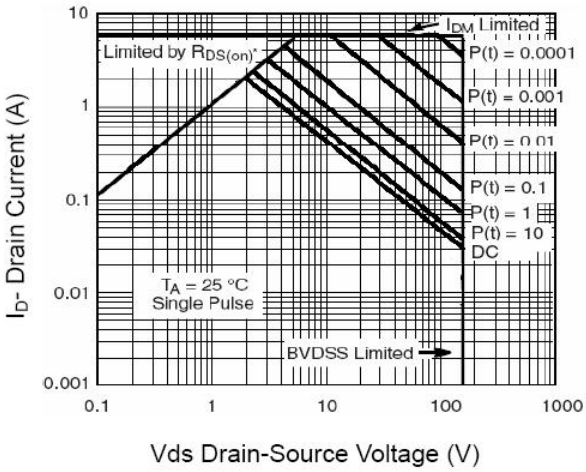

Figure 8 Safe Operation Area

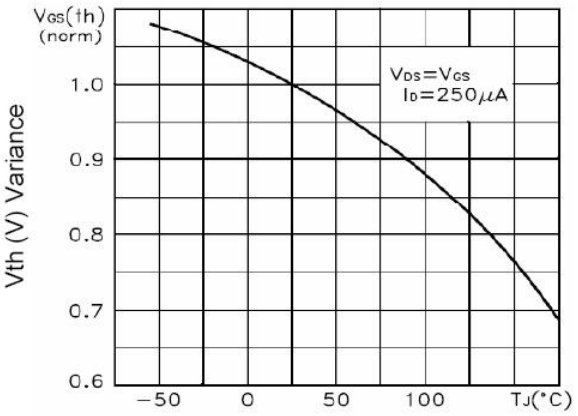

Figure 10 $V_{GS(th)}$ vs Junction Temperature

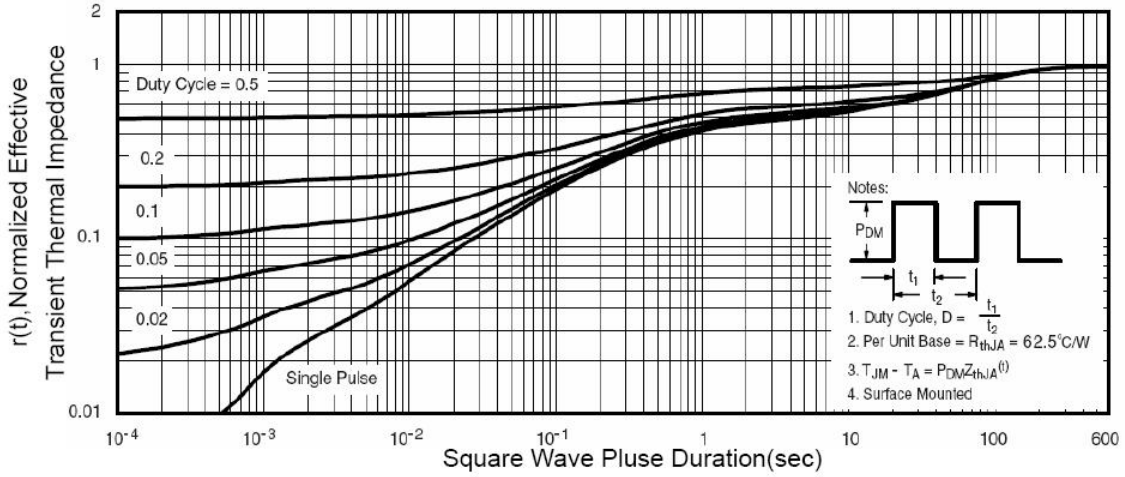

Figure 11 Normalized Maximum Transient Thermal Impedance