

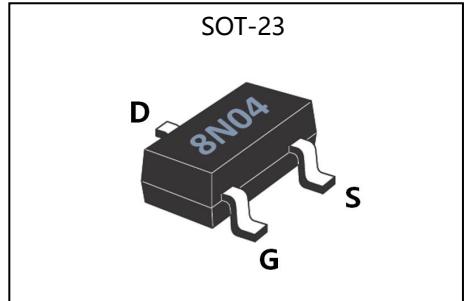
General Description

The GL8N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the RoHS standard.

V_{DSS}	40	V
I_D	8	A
P_D	2	W
$R_{DS(ON)}\text{type}$	18	$\text{m}\Omega$

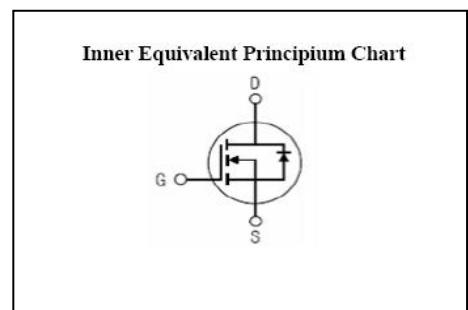
Features

- $R_{DS(ON)} < 22\text{m}\Omega @ V_{GS}=10\text{V}$ (Typ18mΩ)
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Absolute ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	N-Channel	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	8	A
I_{DM}	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	2	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient	62.5	°C/W



GL8N04

GL Silicon N Channel Power MOSFET

Electrical Characteristics (T_c= 25°C unless otherwise specified)

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =40V, V _{GS} =0V, T _a =25°C	--	--	1.0	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+10V	--	--	0.1	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-10V	--	--	-0.1	μA

ON Characteristics^{a3}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =8A	--	18	22	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V

Pulse width tp≤380μs, δ≤2%

Dynamic Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =8A	3	--	--	S
C _{iss}	Input Capacitance		--	415	--	
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =20V f=1.0MHz	--	115	--	pF
C _{rss}	Reverse Transfer Capacitance		--	11	--	

Resistive Switching Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time		--	4.5	--	
t _r	Rise Time	V _{DD} =15V, R _L =2.5Ω	--	3.0	--	
t _{d(OFF)}	Turn-Off Delay Time	V _{GS} =10V, R _G =3Ω	--	14.5	--	ns
t _f	Fall Time		--	3.0	--	
Q _g	Total Gate Charge	V _{DD} =20V, I _D =8A	--	12	--	
Q _{gs}	Gate to Source Charge	V _{GS} =10V	--	3.2	--	nC
Q _{gd}	Gate to Drain ("Miller")Charge		--	3.1	--	



GL8N04

GL Silicon N Channel Power MOSFET

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I _S	Continuous Source Current ^{a2} (Body Diode)		--	--	8	A
V _{SD}	Diode Forward Voltage ^{a3}	I _S =8A, V _{GS} =0V	--	--	1.5	V

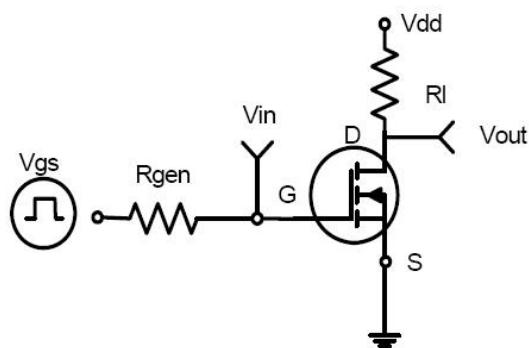
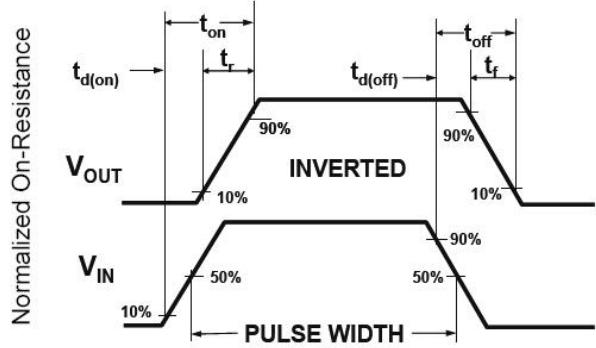
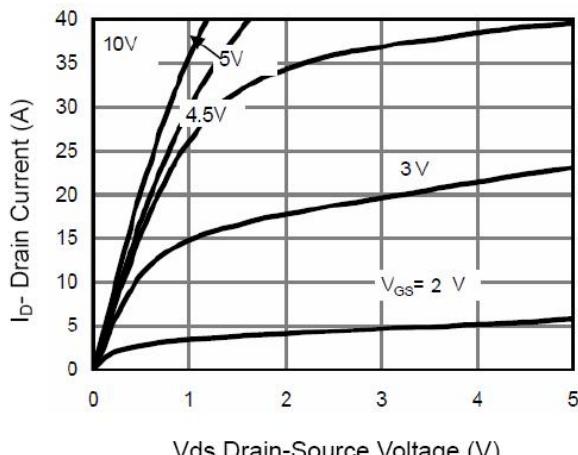
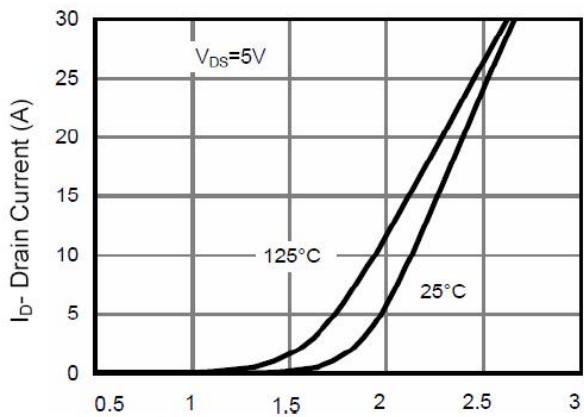
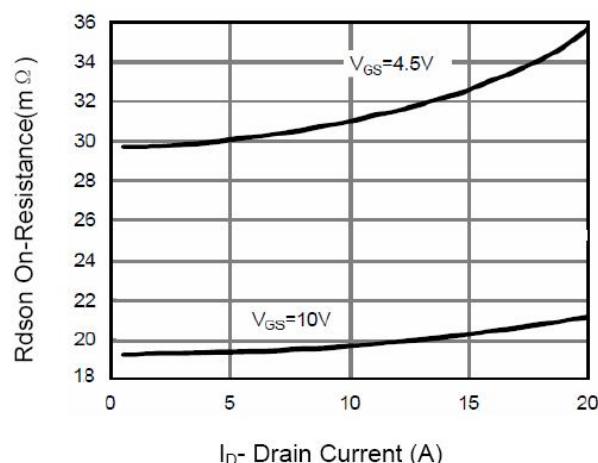
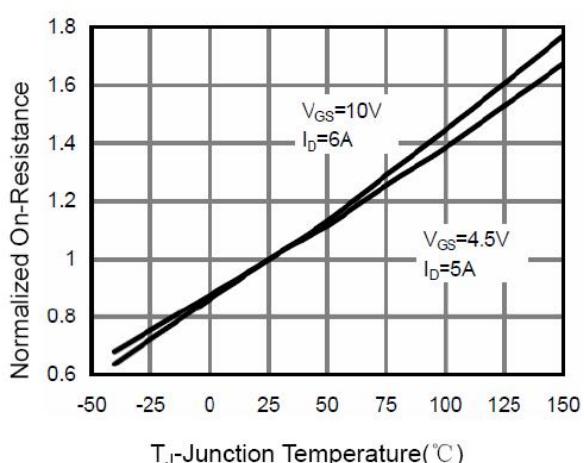
^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2}: Surface Mounted on FR4 Board, t≤10sec.

^{a3}: Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.

^{a4}: Guaranteed by design, not subject to production

^{a5}: EAS condition: T_j=25°C, V_{DD}=15V, V_{GS}=10V, L=1.0mH, R_g=25Ω

Characteristics Curves

Figure 1:Switching Test Circuit

Figure 2:Switching Waveforms

Figure 3 Output Characteristics

Figure 4 Transfer Characteristics

Figure 5 Drain-Source On-Resistance

Figure 6 Drain-Source On-Resistance

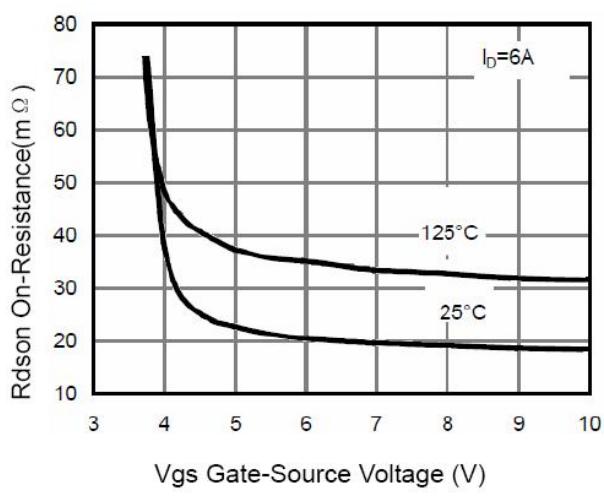
GL Silicon N Channel Power MOSFET


Figure 7 Rdson vs Vgs

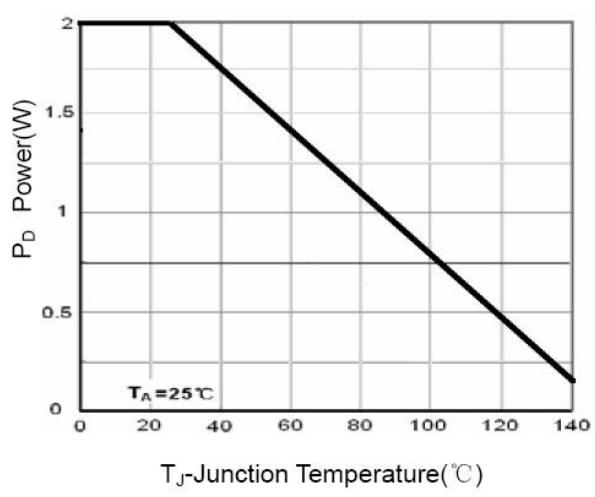


Figure 8 Power Dissipation

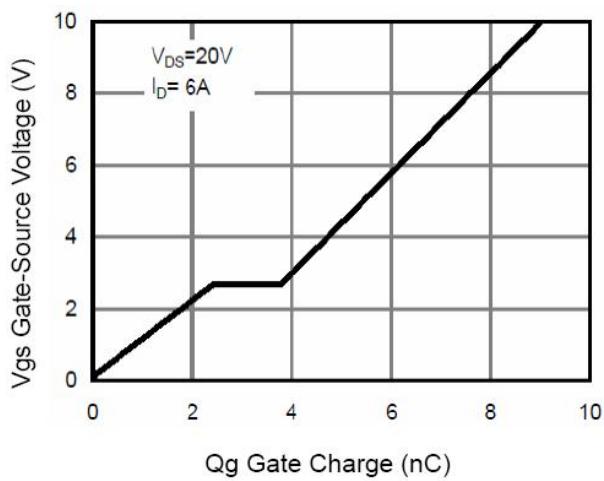


Figure 9 Gate Charge

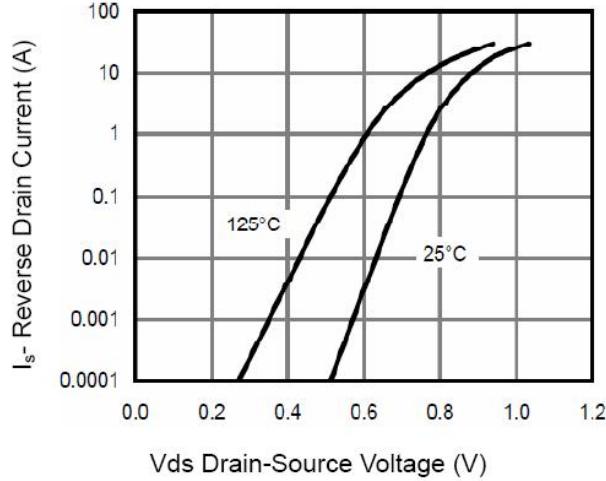


Figure 10 Source- Drain Diode Forward

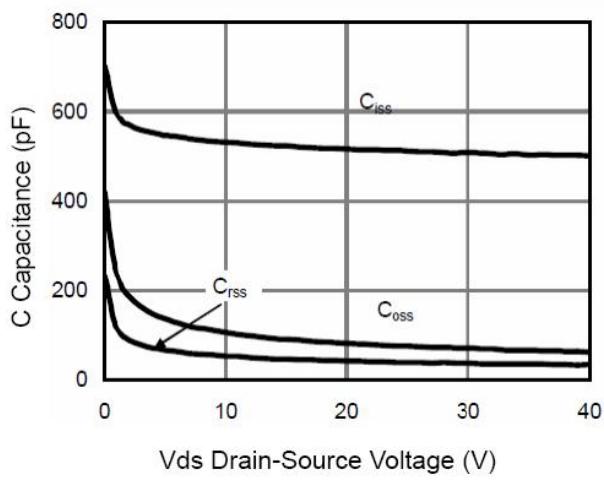


Figure 11 Capacitance vs Vds

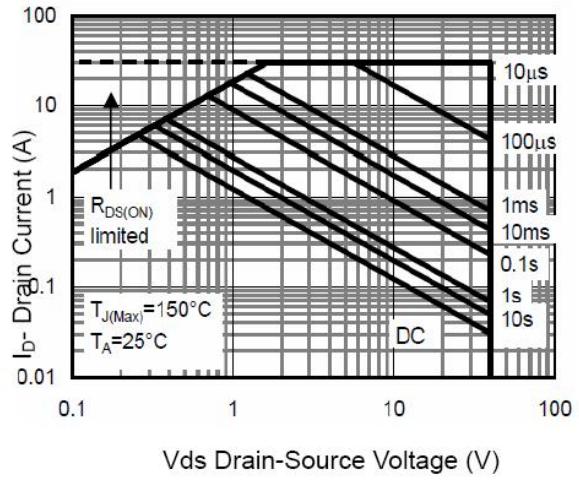


Figure 12 Safe Operation Area

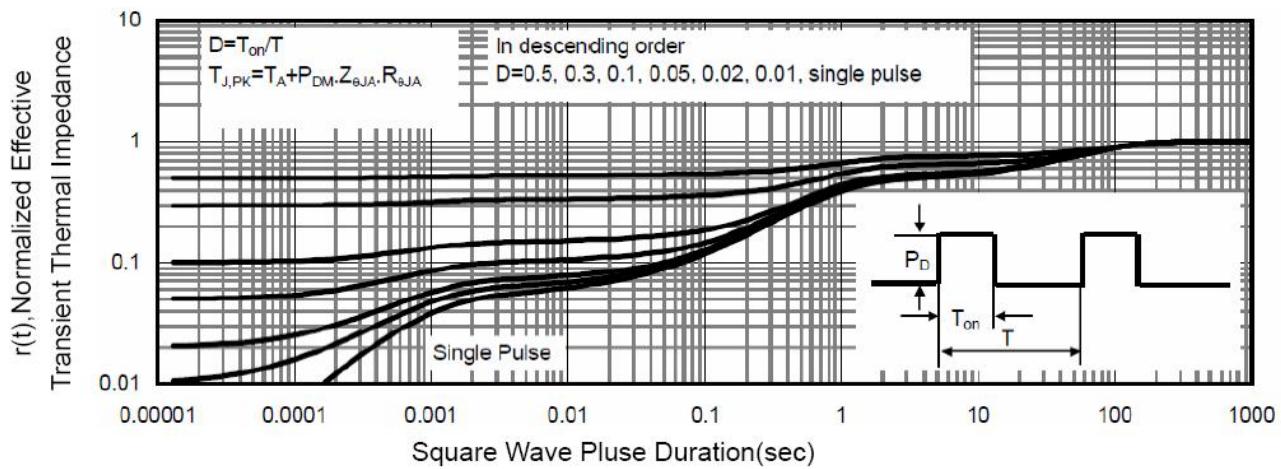


Figure 13 Normalized Maximum Transient Thermal Impedance