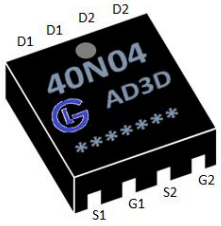
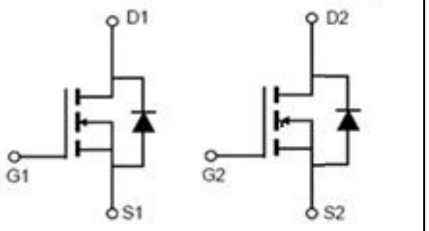
GL40N04AD3D

GL Silicon N-Channel Power MOSFET

V_{DSS}	40	V
I_D	40	A
P_D	40	W
$R_{DS(ON)TYP}$	13	mΩ

DFN3.3×3.3





General Description:

The GL40N04AD3D uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications. The package form is DFN3.3*3.3, which accords with the RoHS standard and two dies in this form.

Features:

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications:

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute (Tc= 25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	40	A
	Continuous Drain Current T_C = 100 °C	24	A
I_{DM}	Pulsed Drain Current	80	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} [a2]	Single Pulse Avalanche Energy	200	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	40	mJ
I_{AR} [a1]	Avalanche Current	6	A
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	40	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics (Tc=25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	40	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	I_D=250uA,Reference25℃	--	0.1	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS}=40V,V_{GS}=0V,T_a=25℃	--	--	1	μA
		V_{DS}=32V,V_{GS}=0V,T_a=125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	13	17	mΩ
		V_{GS}=4.5V,I_D=10A	--	18	25	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	1.7	2.5	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=20V f=1.0MHz	--	960	--	pF
C_{oss}	Output Capacitance		--	100	--	
C_{rss}	Reverse Transfer Capacitance		--	95	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=10A,V_{DD}=20V V_{GS}=10V,R_G=3.0Ω	--	5.5	--	ns
t_r	Rise Time		--	14	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	24.0	--	
t_f	Fall Time		--	12	--	
Q_g	Total Gate Charge	I_D=10A,V_{DD}=20V V_{GS}=10V	--	22	--	nC
Q_{gs}	Gate to Source Charge		--	3	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	5	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	40	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	80	A
V_{SD}	Diode Forward Voltage	I_S=10A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=10A,T_j=25°C	--	30	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/us,V_{GS}=0V	--	40	--	nC
Pulse width tp≤380μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Ambient	3.13	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: EAS condition : Tj=25 ,VDD= ℃ 30V,VG=10V,L=0.5mH,Rg=25Ω

[a3]: I_{SD} =10A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Test Circuit and Waveform

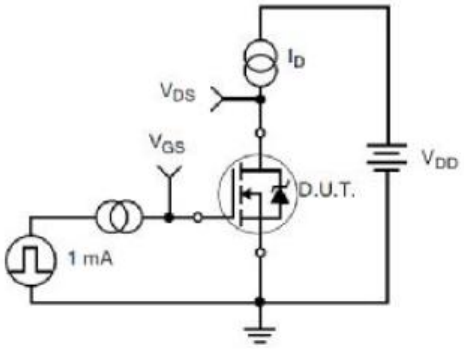


Figure 17. Gate Charge Test Circuit

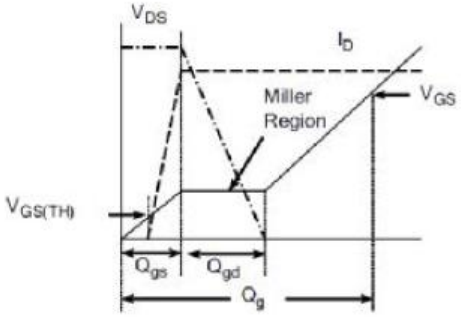


Figure 18. Gate Charge Waveform

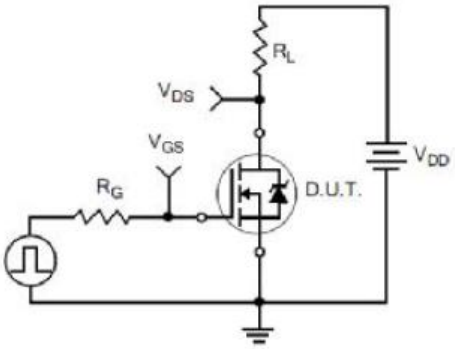


Figure 19. Resistive Switching Test Circuit

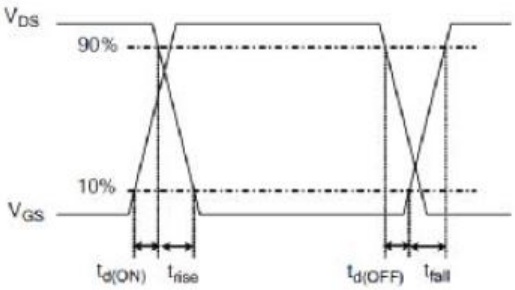


Figure 20. Resistive Switching Waveforms

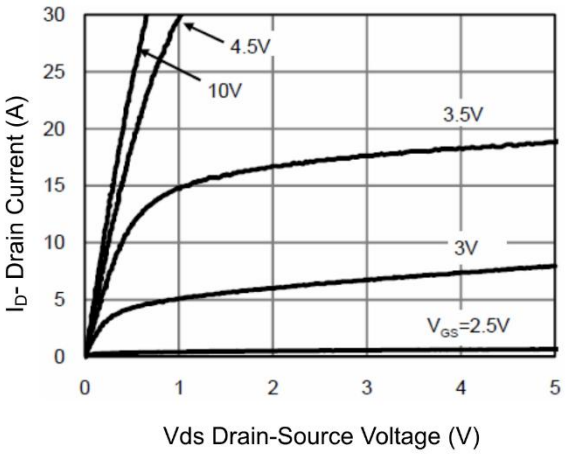


Figure 1 Output Characteristics

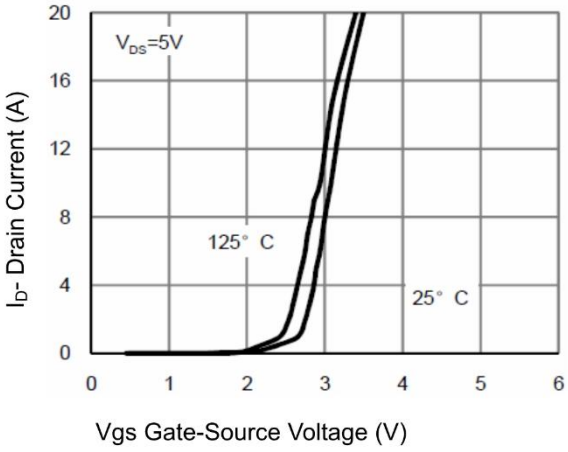


Figure 2 Transfer Characteristics

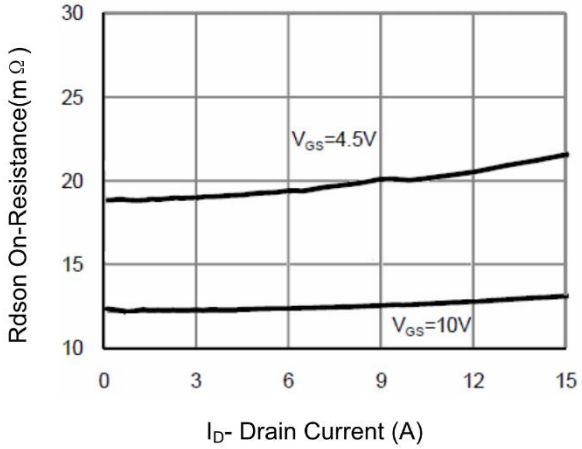


Figure 3 Drain-Source On-Resistance

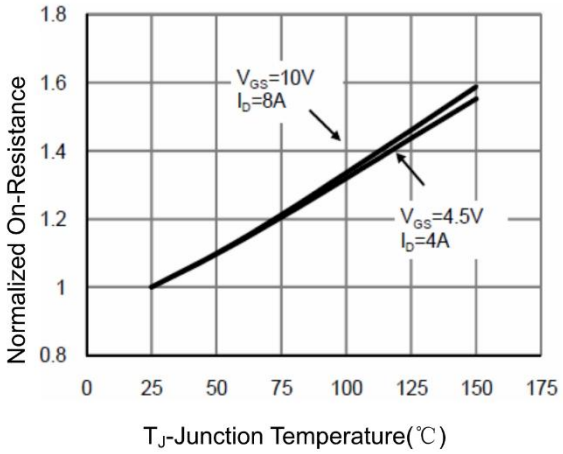


Figure 4 Drain-Source On-Resistance

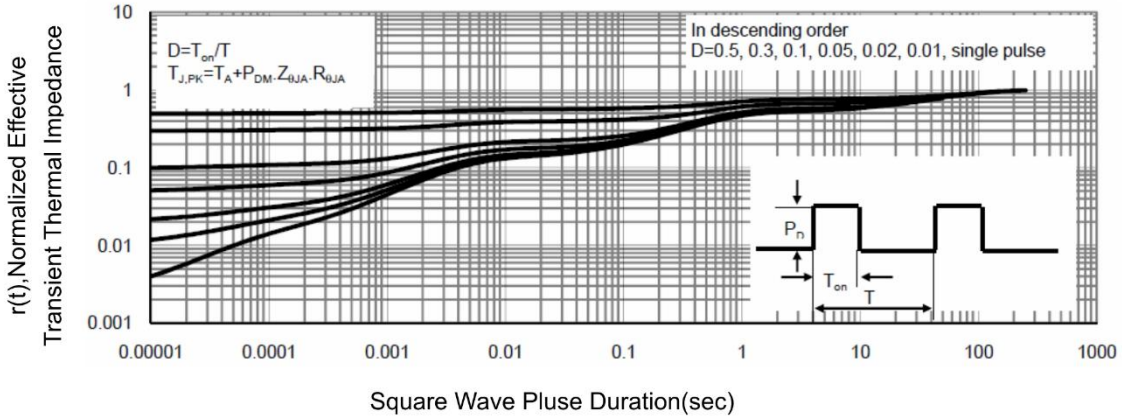


Figure 5 Normalized Maximum Transient Thermal Impedance

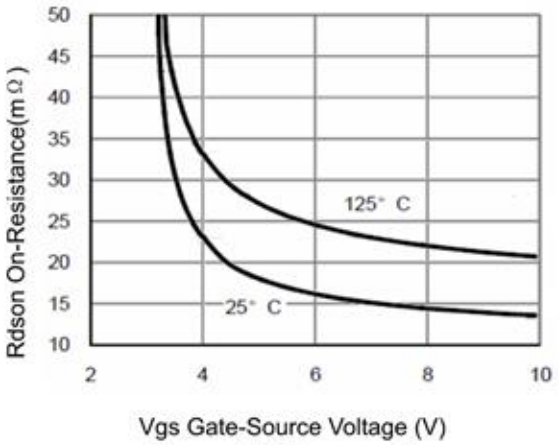


Figure 6 Rdson vs Vgs

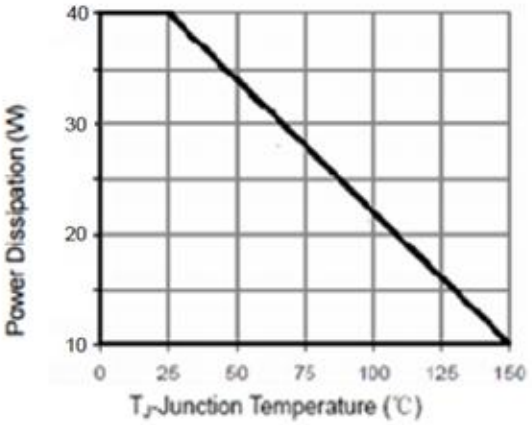


Figure7 Power Dissipation

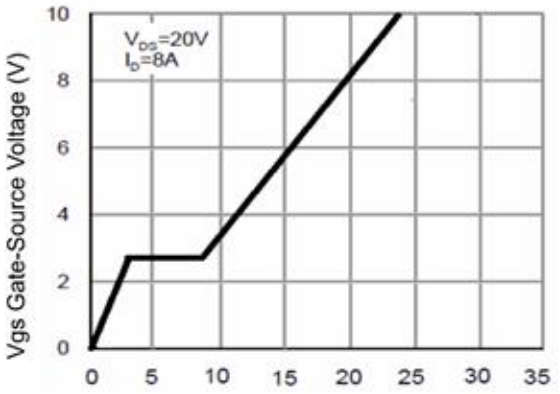


Figure 8 Gate Charge

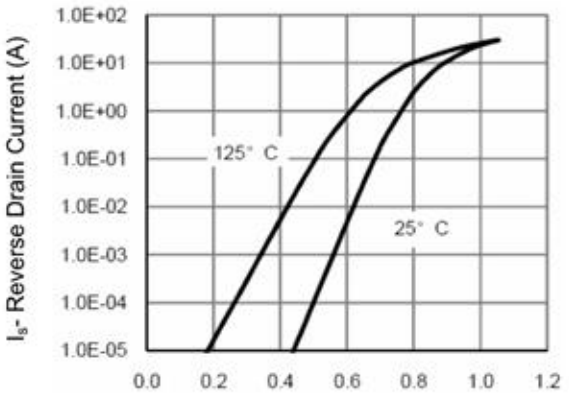


Figure 9 Source- Drain Diode Forward

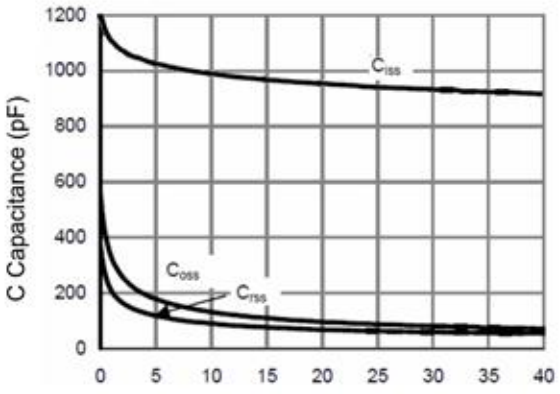


Figure 10 Capacitance vs Vds

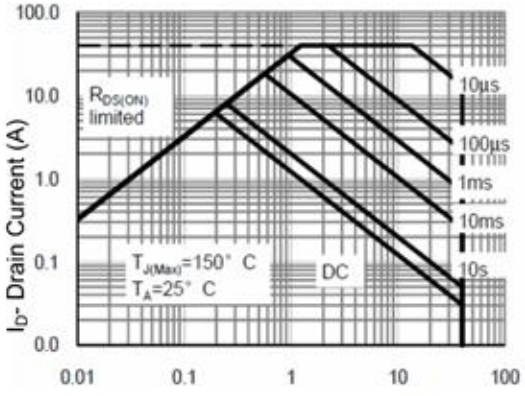


Figure 11 Safe Operation Area