

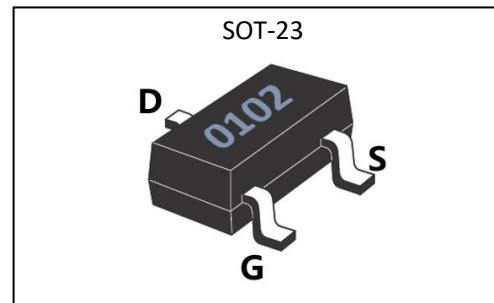
General Description

The GL2N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the RoHS standard.

V_{DSS}	100	V
I_D	2	A
P_D	1.25	W
$R_{DS(ON)type}$	210	$\text{m}\Omega$

Features

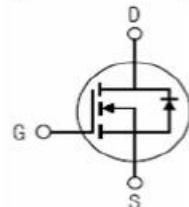
- $R_{DS(ON)} < 265\text{m}\Omega$ @ $V_{GS}=10\text{V}$ (Typ210mΩ)
- High density cell design for ultra low R_{dsn}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Inner Equivalent Principium Chart



Absolute (Tc=25°C unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	2	A
I_{DM}	Pulsed Drain Current	5	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	1.25	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	175, -55 to 175	°C



GL2N10

GL Silicon N-Channel Power MOSFET

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified):

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}, T_a=25^\circ\text{C}$	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20\text{V}$	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20\text{V}$	--	--	-0.1	μA

ON Characteristics^{a3}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10\text{V}, I_D=1\text{A}$	--	--	265	$\text{m}\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.2	--	2.5	V

Pulse width $t_p \leq 380\mu\text{s}, \delta \leq 2\%$

Dynamic Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=1\text{A}$	1	--	--	S
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}$	--	190	--	pF
C_{oss}	Output Capacitance	$f=1.0\text{MHz}$	--	22	--	
C_{rss}	Reverse Transfer Capacitance		--	13	--	

Resistive Switching Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=50\text{V}, I_D=1.3\text{A}, R_L=39\Omega$	--	6	--	ns
t_r	Rise Time		--	10	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	10	--	
t_f	Fall Time		--	6	--	
Q_g	Total Gate Charge	$V_{DD}=50\text{V}, I_D=1.3\text{A}$	--	5.2	--	nC
Q_{gs}	Gate to Source Charge		--	0.75	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	1.4	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_s	Continuous Source Current ^{a2} (Body Diode)		--	--	2	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_s=1.3\text{A}, V_{GS}=0\text{V}$	--	--	1.2	V

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Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient ^{a2}	100	°C/W

^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.

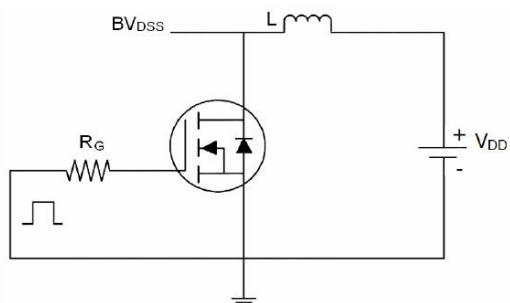
^{a2}: Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

^{a3}: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

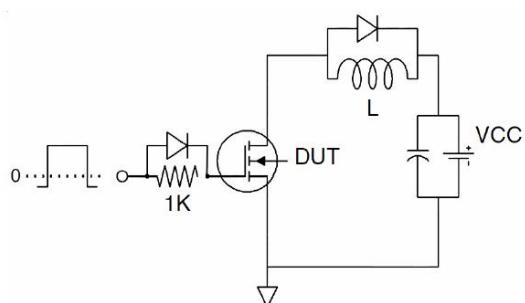
^{a4}: Guaranteed by design, not subject to production

Test circuit

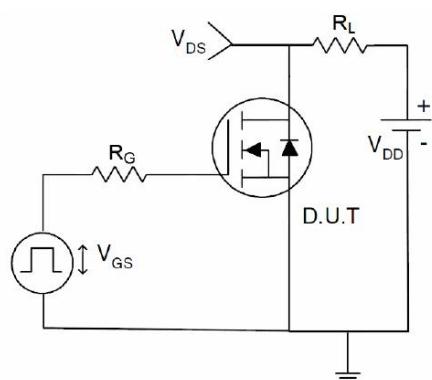
1) EAS test Circuit



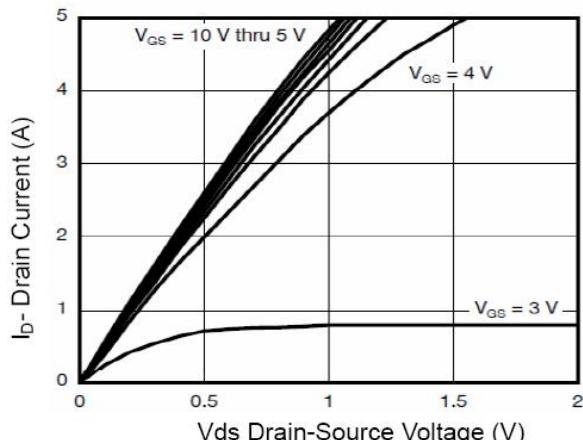
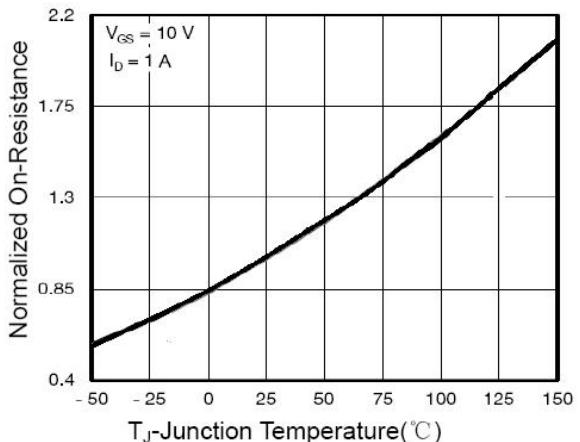
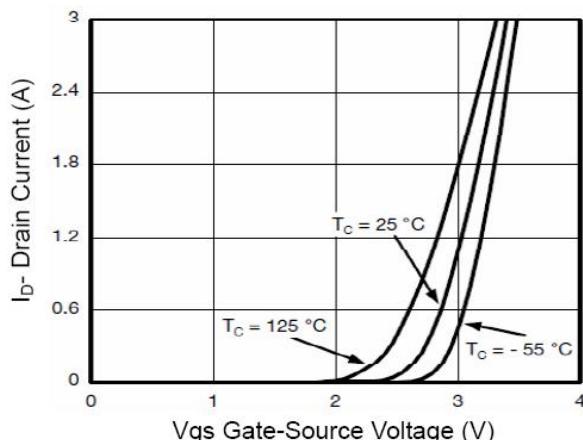
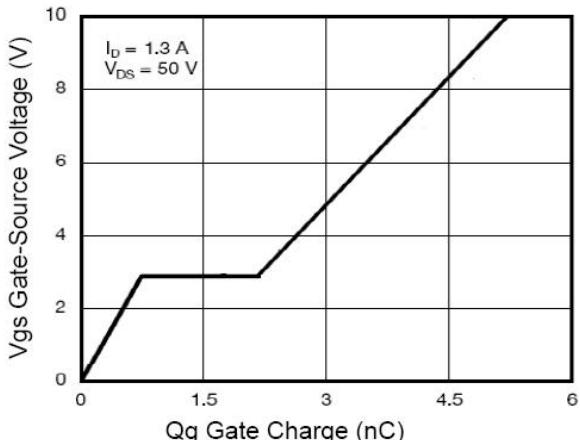
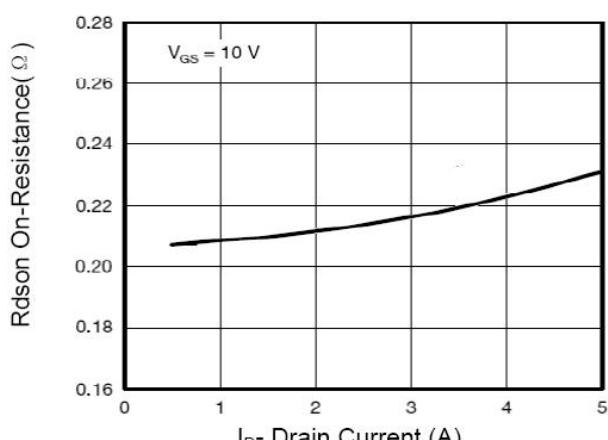
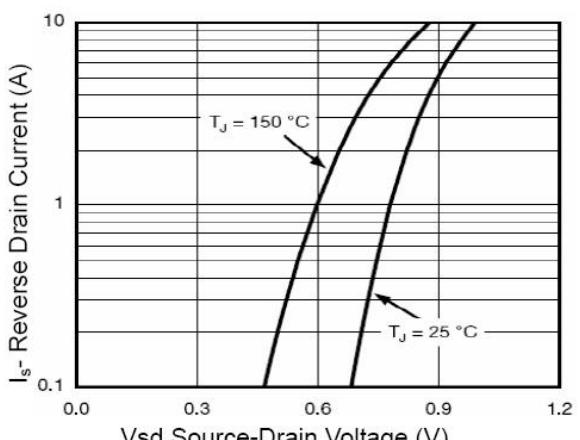
2) Gate charge test Circuit

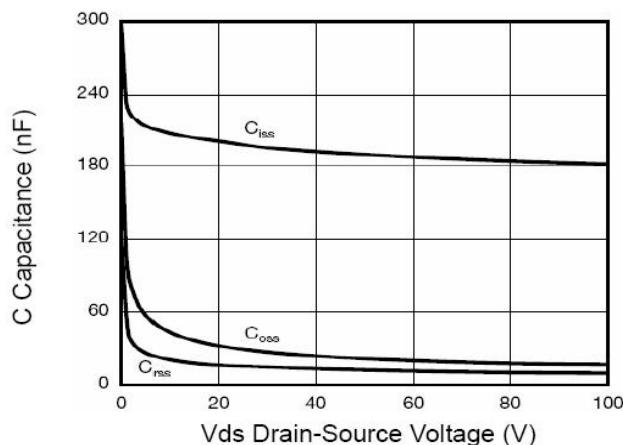
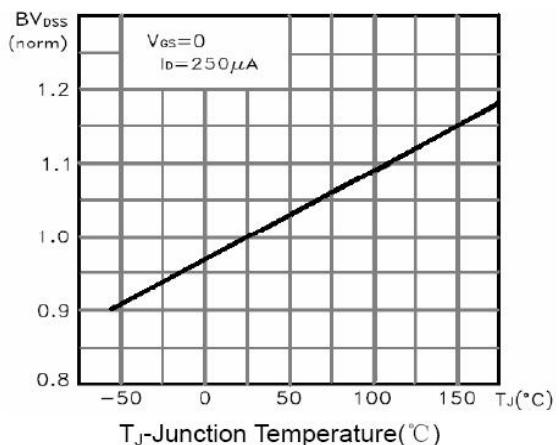
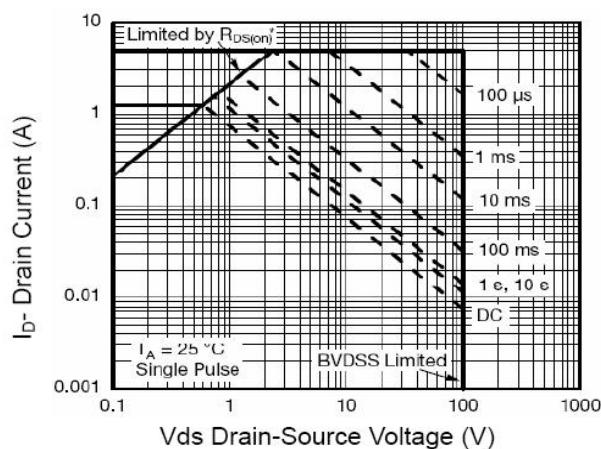
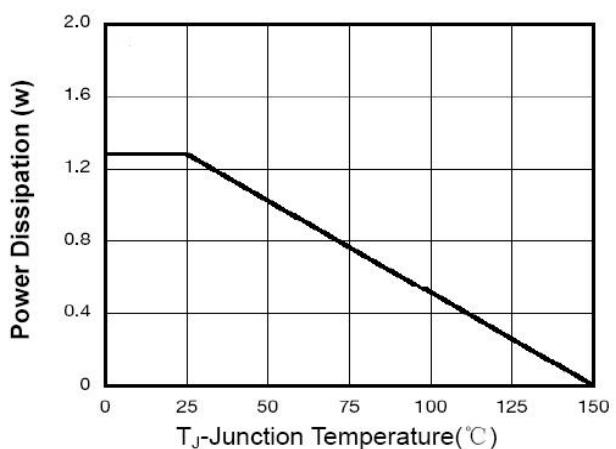
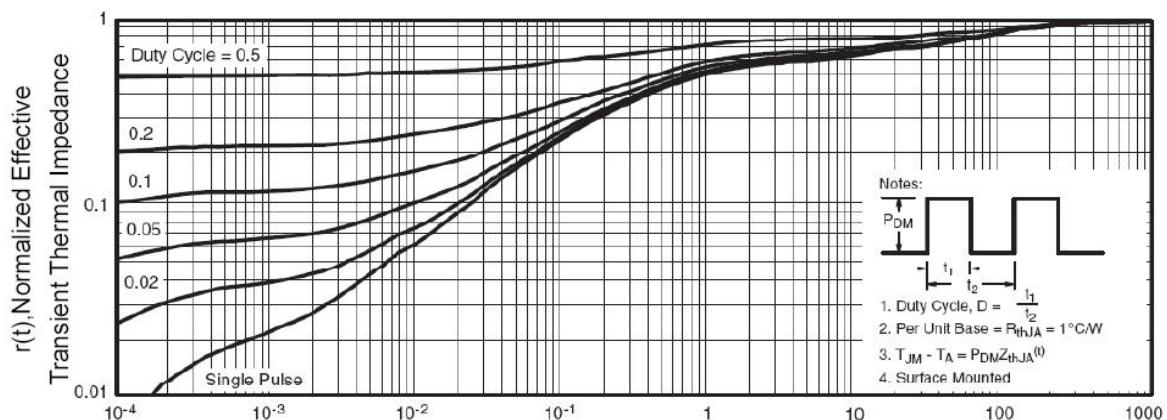


3) Switch Time Test Circuit



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Characteristics Curve

Figure 1 Output Characteristics

Figure 4 Rdson-JunctionTemperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson-Drain Current

Figure 6 Source- Drain Diode Forward

GL Silicon N-Channel Power MOSFET

Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 Power De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance