



GL40N10A4

GL Silicon N-Channel Power MOSFET

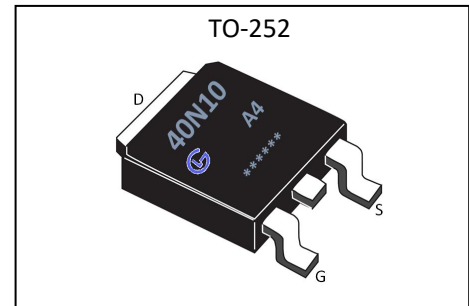
General Description

The GL40N10A4 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TO-251, which accords with the RoHS standard.

V_{DSS}	100	V
I_D	40	A
P_D	100	W
$R_{DS(ON)type}$	12	m Ω

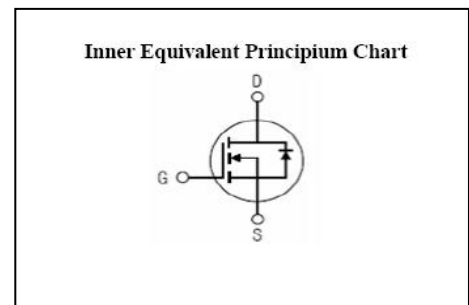
Features

- $R_{DS(ON)} < 16m\Omega$ @ $V_{GS}=10V$ (Typ12m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Absolute (Tc= 25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	40	A
I_{DM}	Pulsed Drain Current	160	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	100	W
	Derating factor	0.8	W/°C
E_{AS}	Single pulse avalanche energy ^{a5}	520	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range	175, -55 to 175	°C



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Electrical Characteristics (Tc= 25°C unless otherwise specified)

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =100V, V _{GS} = 0V, T _a =25°C	--	--	1.0	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} = +20V	--	--	0.1	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} = -20V	--	--	-0.1	μA

ON Characteristics^{a3}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =20A	--	12	16	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	--	2.5	V

Pulse width tp≤380μs, δ≤2%

Dynamic Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Transconductance	V _{DS} =25V, I _D =28A	32	--	--	S
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V f=1.0MHz	--	1133	--	pF
C _{oss}	Output Capacitance		--	70	--	
C _{rss}	Reverse Transfer Capacitance		--	71	--	

Resistive Switching Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	--	5	--	ns
t _r	Rise Time		--	4	--	
t _{d(OFF)}	Turn-Off Delay Time		--	16	--	
t _f	Fall Time		--	5	--	
Q _g	Total Gate Charge	V _{DD} =30V, I _D =30A V _{GS} =10V	--	23	--	nC
Q _{gs}	Gate to Source Charge		--	5	--	
Q _{gd}	Gate to Drain ("Miller") Charge		--	6.5	--	



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Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S=28A, V_{GS}=0V$	--	--	1.2	V

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case ^{a2}	0.783	°C/W

^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2}: Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

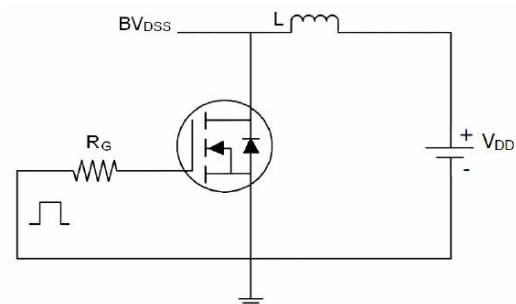
^{a3}: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

^{a4}: Guaranteed by design, not subject to production

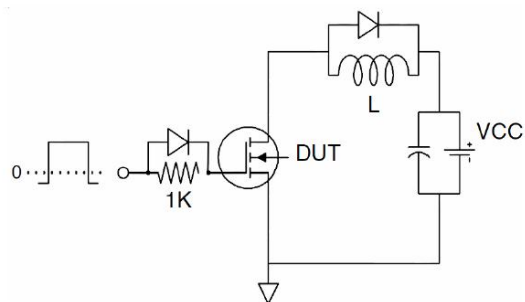
^{a5}: EAS condition: $T_j=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuits

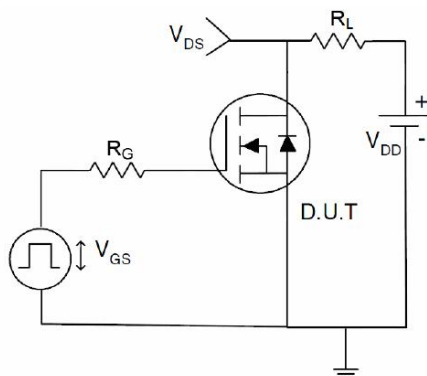
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Characteristics Curves

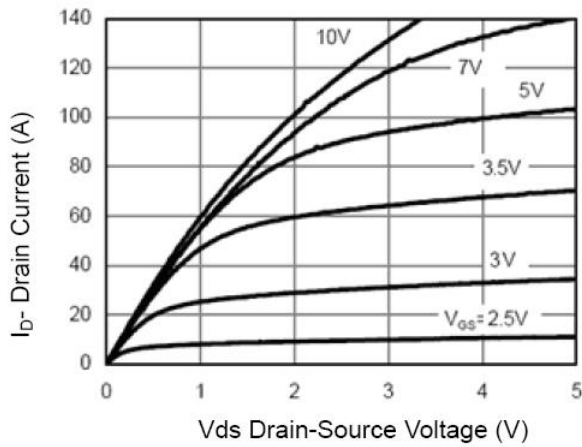


Figure 1 Output Characteristics

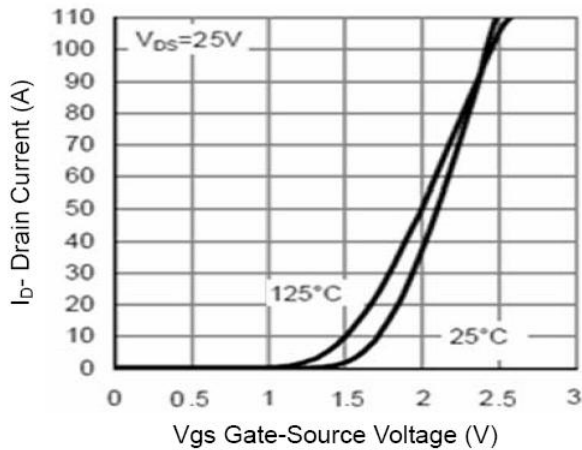


Figure 2 Transfer Characteristics

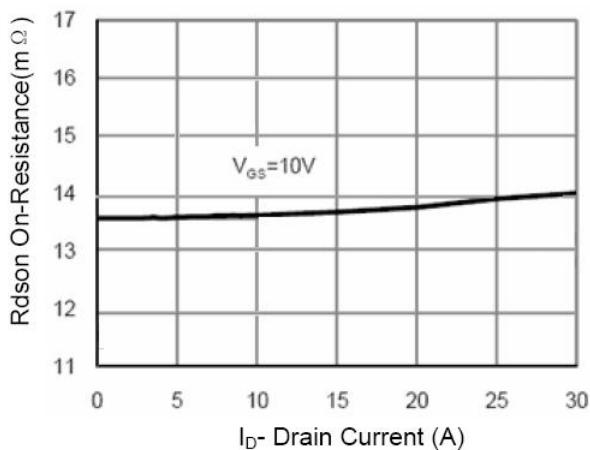


Figure 3 Rdson- Drain Current

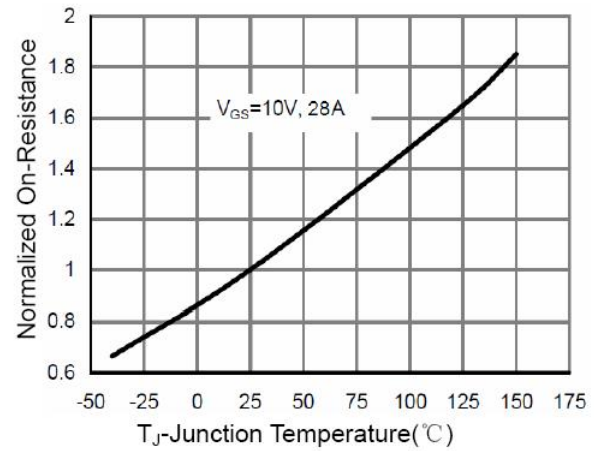


Figure 4 Rdson-Junction Temperature

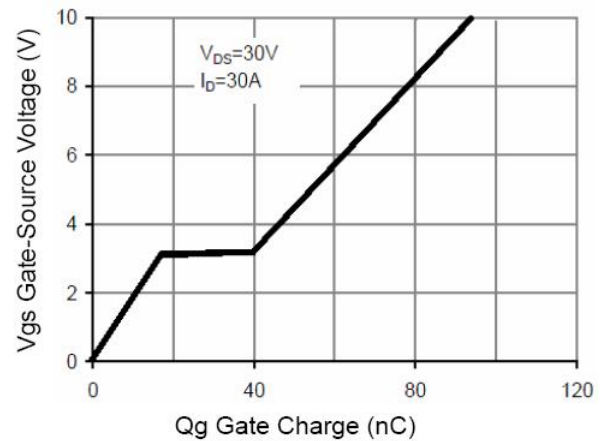


Figure 5 Gate Charge

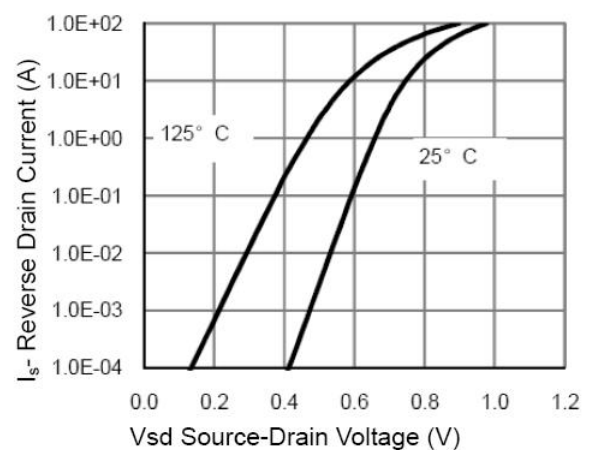


Figure 6 Source- Drain Diode Forward

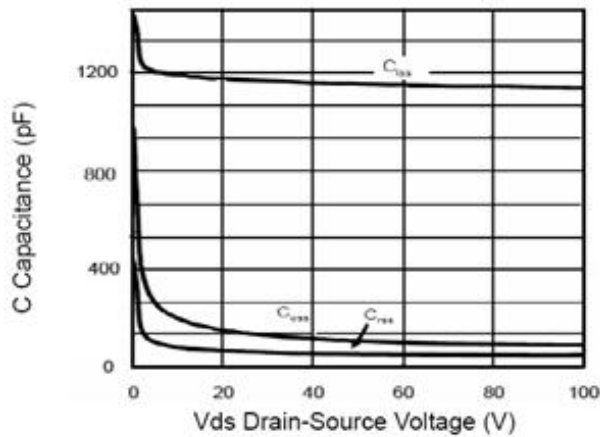


Figure 7 Capacitance vs Vds

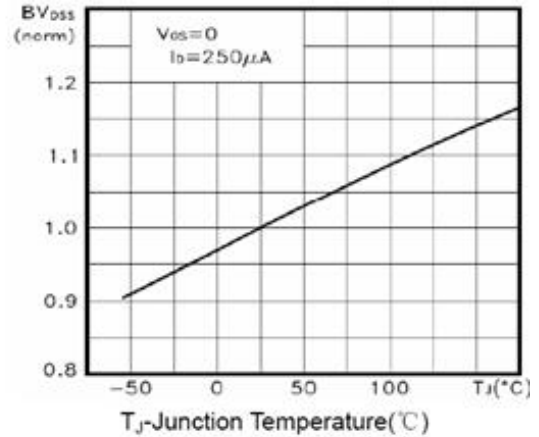


Figure 9 BV_{DSS} vs Junction Temperature

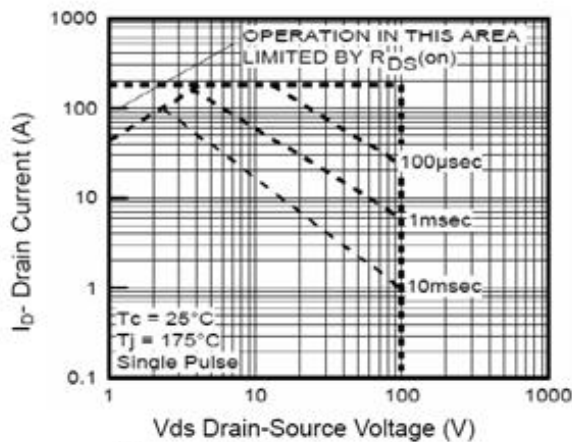


Figure 8 Safe Operation Area

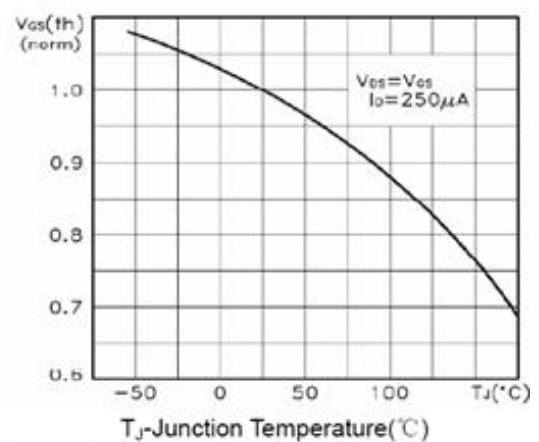


Figure 10 $V_{GS(th)}$ vs Junction Temperature

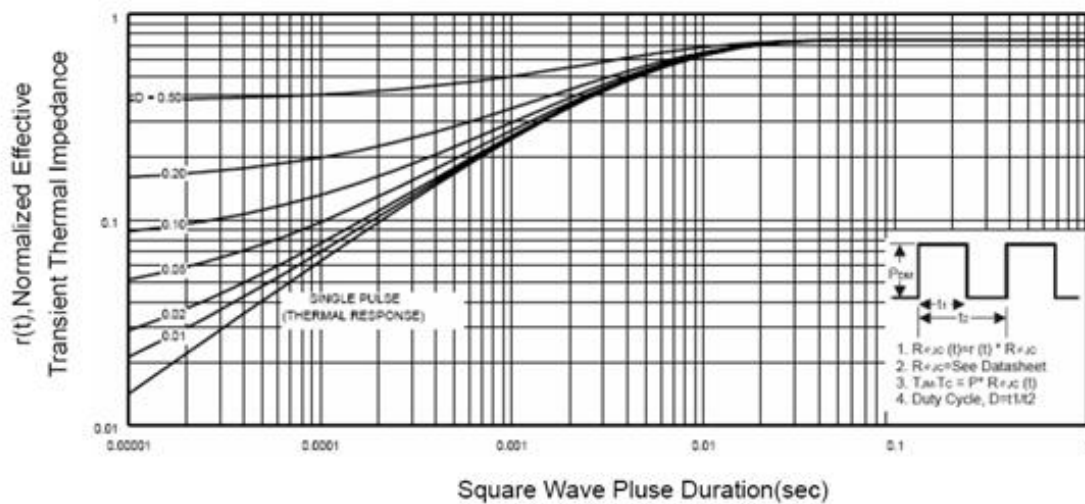


Figure 11 Normalized Maximum Transient Thermal Impedance