GL100N40A64FD

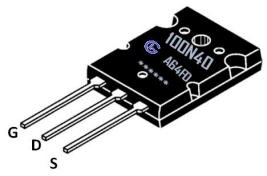
Silicon N-Channel Power MOSFET Integrated FRD

V_{DSS}	400	V
I_D	100	A
$P_D(T_C=25℃)$	700	W
$R_{DS(ON)TYPE}$	34	mΩ

General Description:

GL100N40A64FD, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit . The package form is TO-264, which accords with the RoHS standard.

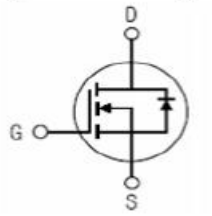
TO-264



Features:

- Fast Switching
- Low ON Resistance
- Low Gate Charge Minimize Switching loss
- Fast Recovery Body Diode
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

Absolute (Tc= 25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	400	V
I_D	Continuous Drain Current	100	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	250	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy	2500	mJ
dv/dt	Peak Diode Recovery dv/dt	10	V/ns
P_D	Power Dissipation	700	W
	Derating Factor above 25°C	5.6	W/℃
T_J,T_{stg}	Operating Junction and Storage Temperature Range	150,–55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃
T_{PAK}	Leads at 0.63 in(1.6mm) from Case for 10S, Package Body for 10S.	260	

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	400	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=400V, V_{GS}=0V,T_a=25℃	--	--	10	μA
		V_{DS}=320V, V_{GS}=0V,T_a=125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	200	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-200	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=50A	--	34	40	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=500μA	3.0	--	5.0	V
g_{fs}	Forward Transconductance	V_{DS}=10V,I_D=32A	45	--	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	12000	--	pF
C_{oss}	Output Capacitance		--	1150	--	
C_{rss}	Reverse Transfer Capacitance		--	150	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=50A,V_{DD}=200V V_{GS}=10V,R_g=3.3Ω	--	36	--	ns
t_r	Rise Time		--	28	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	130	--	
t_f	Fall Time		--	30	--	
Q_g	Total Gate Charge	I_D=50A,V_{DD}=200V V_{GS}=10V	--	220	--	nC
Q_{gs}	Gate to Source Charge		--	50	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	110	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	100	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	250	A
V_{SD}	Diode Forward Voltage	I_S=100A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=50A,T_j=25℃	--	130	200	ns
Q_{rr}	Reverse Recovery Charge	di/dt=100A/μs,V_R=100V	--	3.3	--	μC
*Pulse width tp≤380μs,δ≤2%						

Thermal Characteristics			
Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.18	℃/ W

Characteristics Curve:

Fig. 1. Output Characteristics @ 25°C

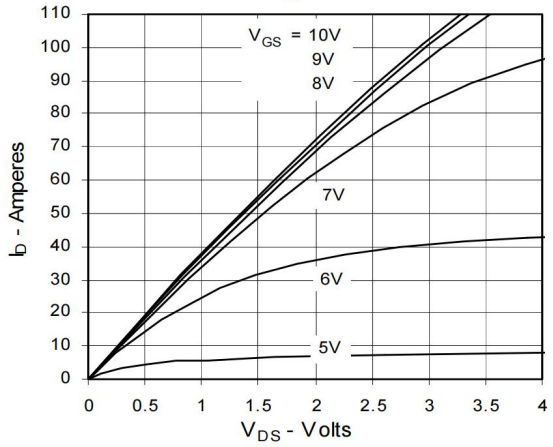


Fig. 2. Extended Output Characteristics @ 25°C

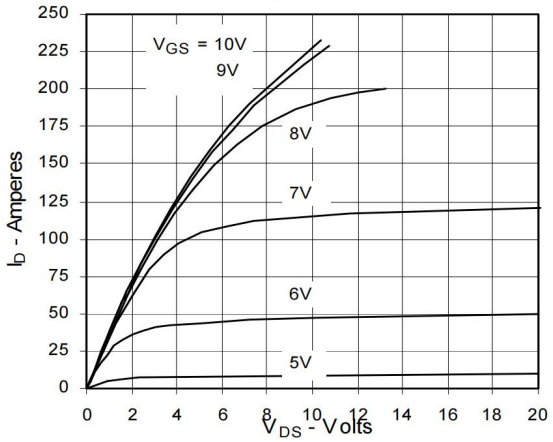


Fig. 3. Output Characteristics @ 125°C

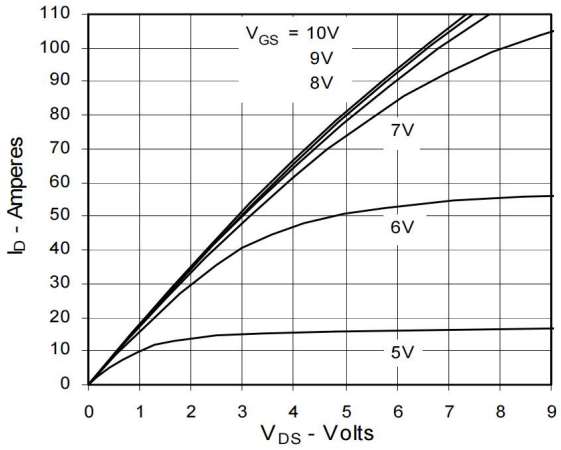


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

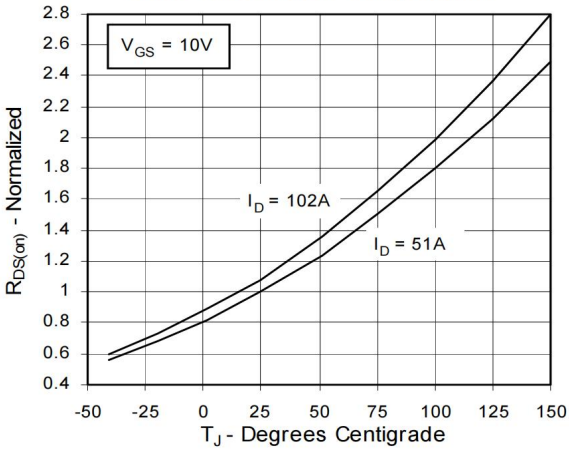


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

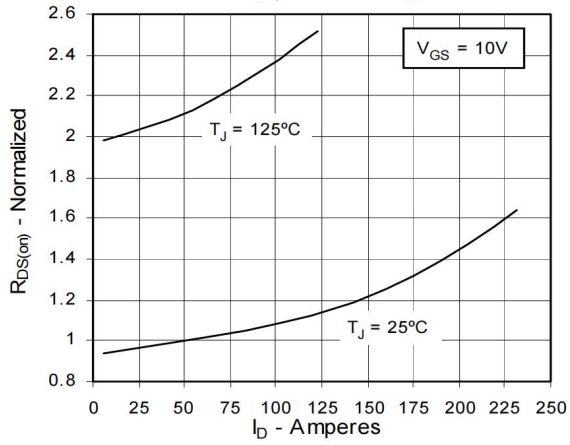


Fig. 6. Drain Current vs. Case Temperature

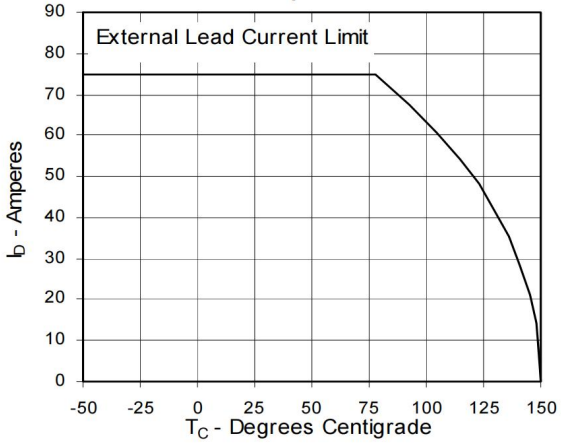


Fig. 7. Input Admittance

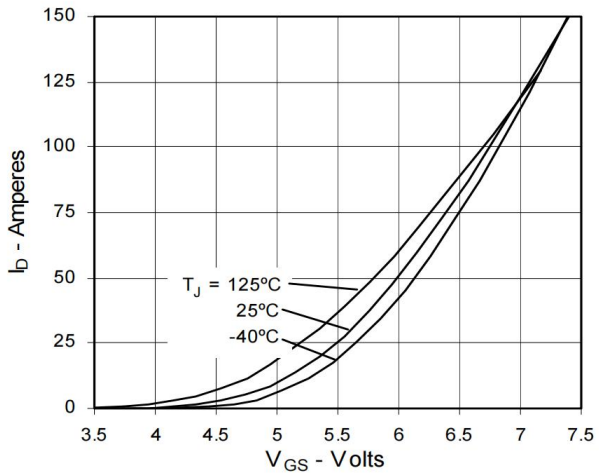


Fig. 8. Transconductance

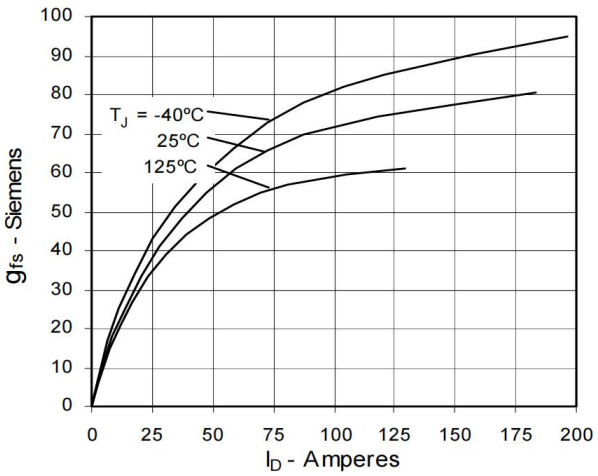


Fig. 9. Source Current vs. Source-To-Drain Voltage

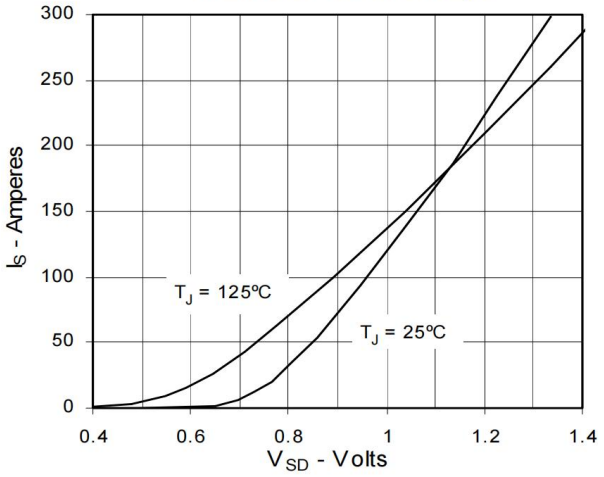


Fig. 10. Gate Charge

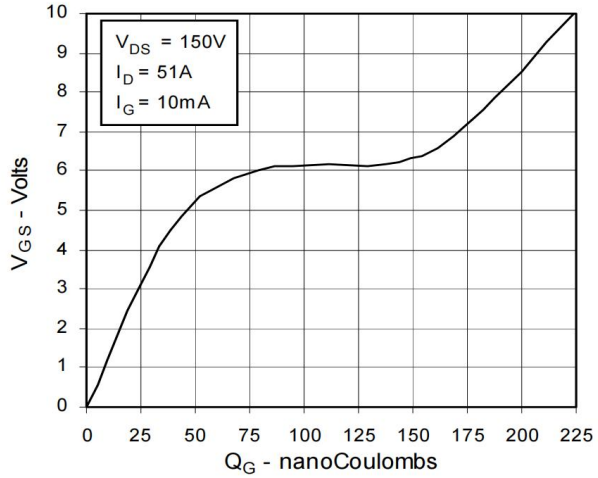


Fig. 11. Capacitance

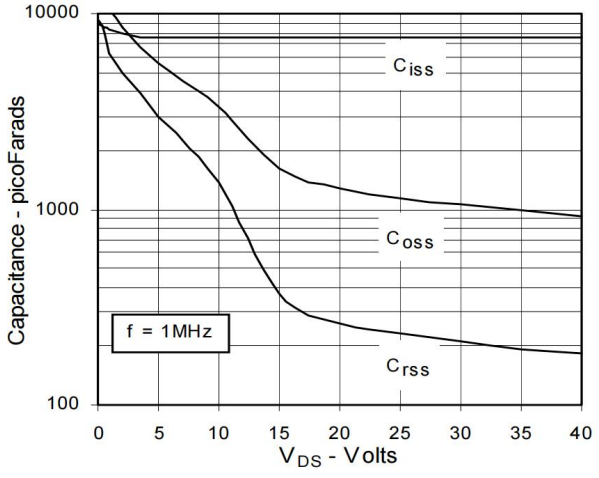


Fig. 12. Forward-Bias Safe Operating Area

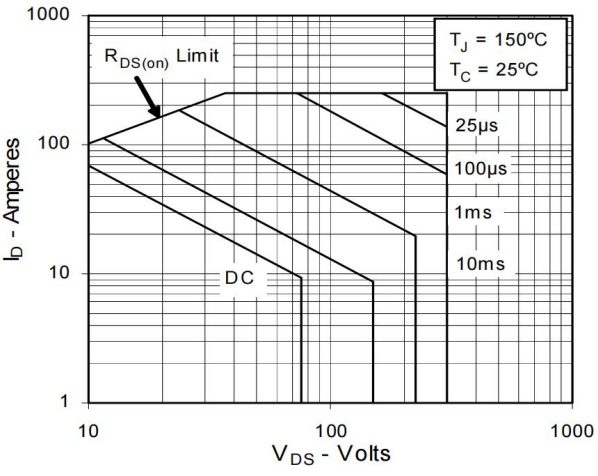


Fig. 13. Maximum Transient Thermal Resistance