

General Description:

GL5N50A8, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220, which accords with the RoHS standard.

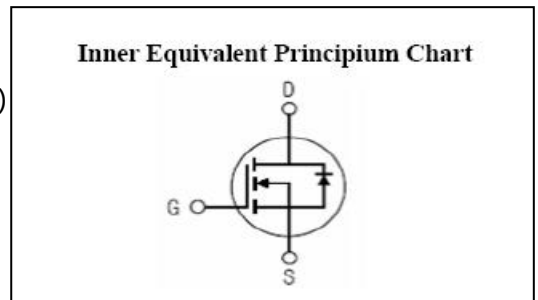
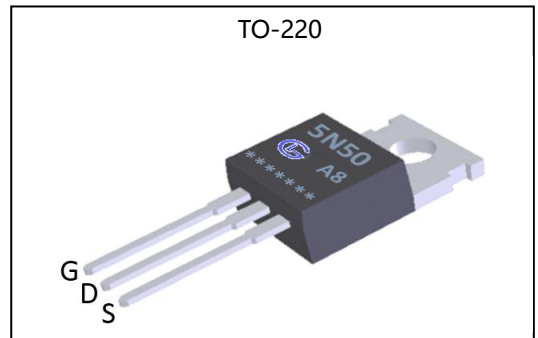
Features:

- Fast Switching
- Low ON Resistance($R_{ds(on)} \leq 1.5\Omega$)
- Low Gate Charge (Typical Data:14.5nC)
- Low Reverse transfer capacitances(Typical:3.5pF)
- 100% Single Pulse avalanche energy Test

Applications:

- Power switch circuit of adaptor and charger

V_{DSS}	500	V
I_D	5	A
$P_D(T_C=25^\circ C)$	75	W
$R_{DS(ON).TYP.}$	1.2	Ω



Absolute (Tc=25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	5	A
	Continuous Drain Current $T_C=100^\circ C$	3.1	A
I_{DM}^{a1}	Pulsed Drain Current	20	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	260	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	75	W
	Derating Factor above $25^\circ C$	0.6	W/ $^\circ C$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ C$
T_L	Maximum Temperature for Soldering	300	$^\circ C$

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.67	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ C/W$



GL5N50A8

Silicon N-Channel Power MOSFET

Electrical Characteristics (Tc= 25°C unless otherwise specified):

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A$, Reference 25°C	--	0.6	--	V/°C
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=500V, V_{GS}=0V, T_a=25^\circ C$	--	--	1.0	μA
		$V_{DS}=400V, V_{GS}=0V, T_a=125^\circ C$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=2.5A$	--	1.2	1.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=2.5A$	--	4.0	--	S

Pulse width < 380 μ s; duty cycle < 2%.

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	610	--	pF
C_{oss}	Output Capacitance		--	53	--	
C_{rss}	Reverse Transfer Capacitance		--	3.5	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=5A, V_{DD}=250V$ $V_{GS}=10V, R_g=10\Omega$	--	14	--	ns
t_r	Rise Time		--	16	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	32	--	
t_f	Fall Time		--	11	--	
Q_g	Total Gate Charge	$I_D=5A, V_{DD}=250V$ $V_{GS}=10V$	--	14.5	--	nC
Q_{gs}	Gate to Source Charge		--	3	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	6.5	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	5	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	20	A
V_{SD}	Diode Forward Voltage	$I_S = 5A, V_{GS} = 0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S = 5A, T_J = 25^\circ C$	--	310	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100A/\mu s, V_{GS} = 0V$	--	1300	--	nC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $L = 10mH$, $I_D = 7.3A$, Start $T_J = 25^\circ C$

a3: $I_{SD} = 5A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS}$, Start $T_J = 25^\circ C$

Test Circuit and Waveform:

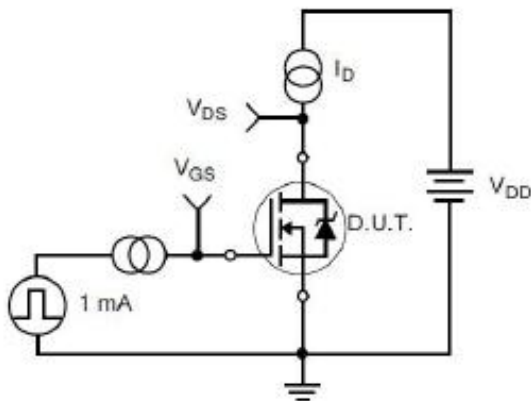


Figure 17. Gate Charge Test Circuit

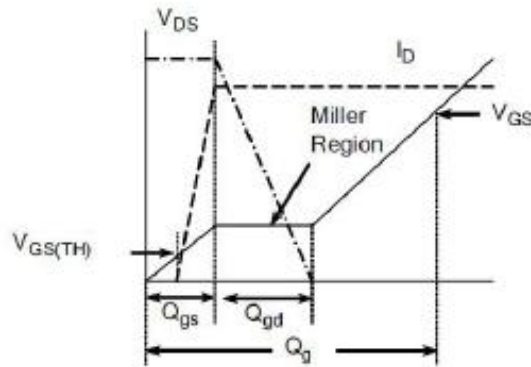


Figure 18. Gate Charge Waveform

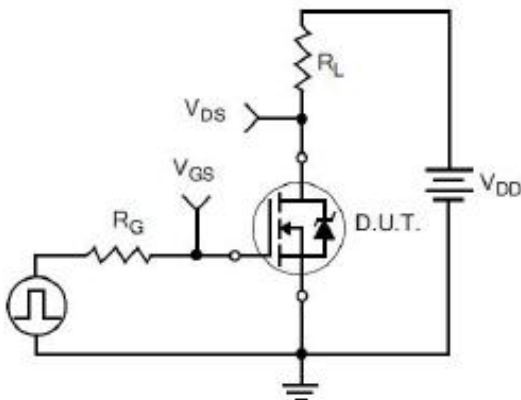


Figure 19. Resistive Switching Test Circuit

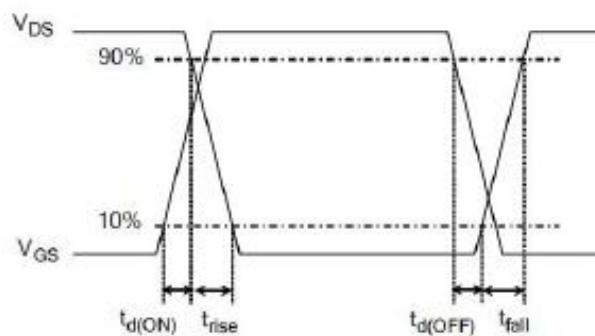


Figure 20. Resistive Switching Waveforms

Characteristics Curve:

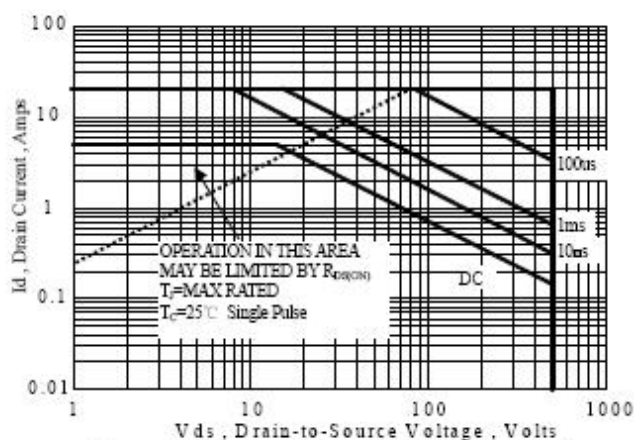


Figure 1 Maximum Forward Bias Safe Operating Area

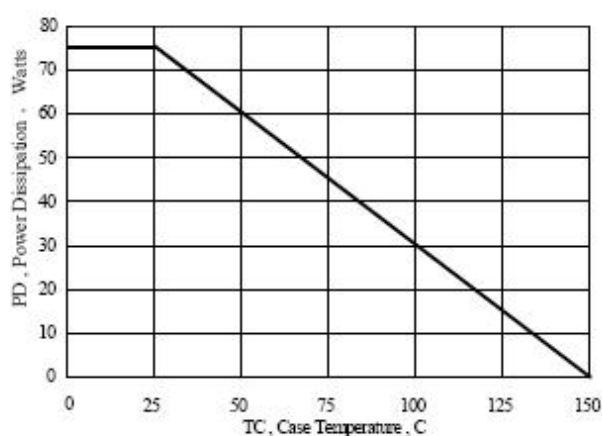


Figure 2 Maximum Power Dissipation vs Case Temperature

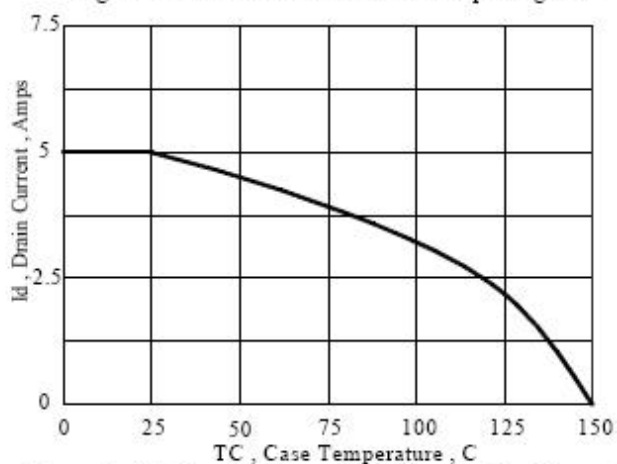


Figure 3 Maximum Continuous Drain Current vs Case Temperature

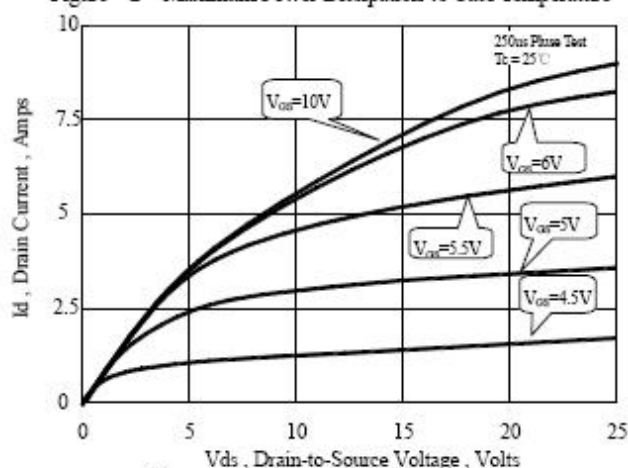


Figure 4 Typical Output Characteristics

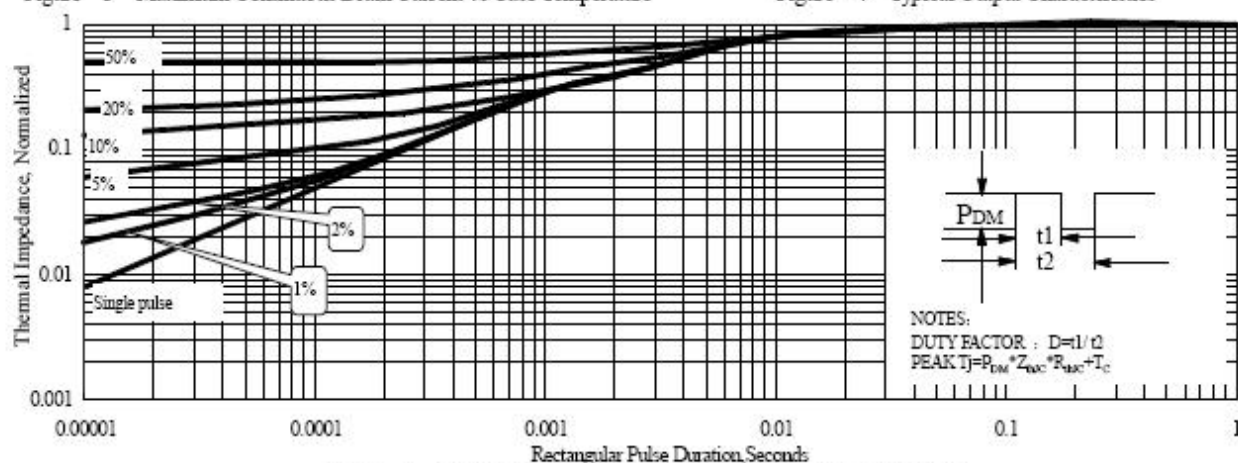


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

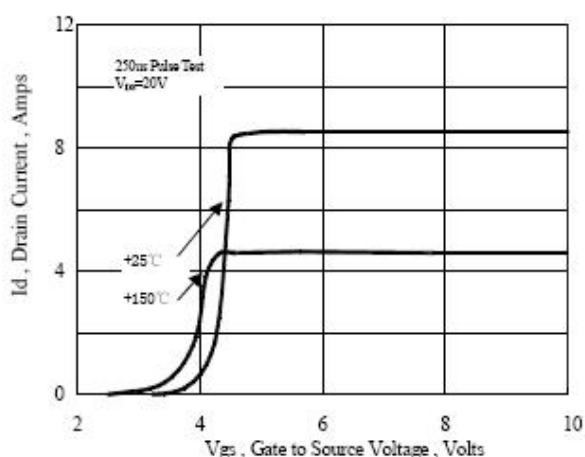


Figure 6 Typical Transfer Characteristics

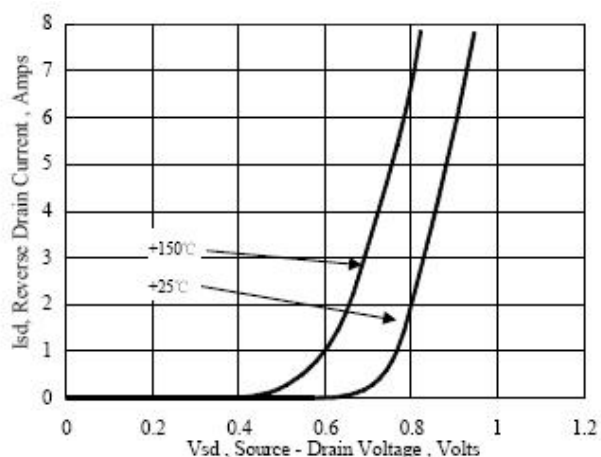


Figure 7 Typical Body Diode Transfer Characteristics

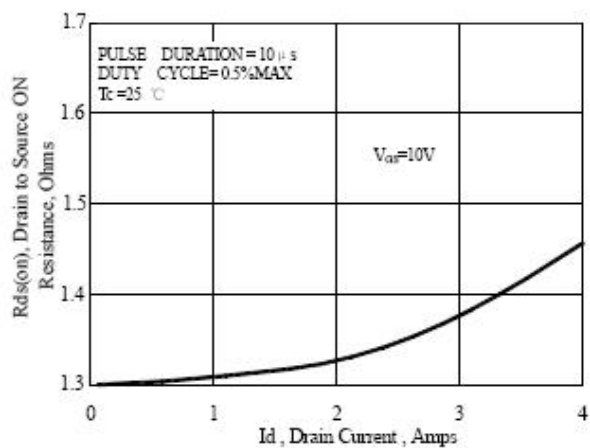


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

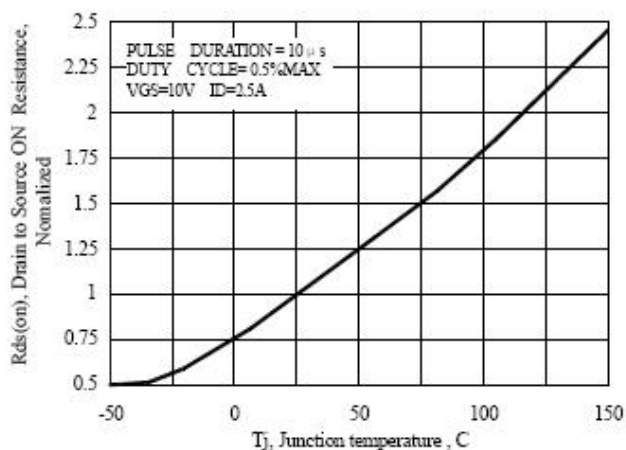


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

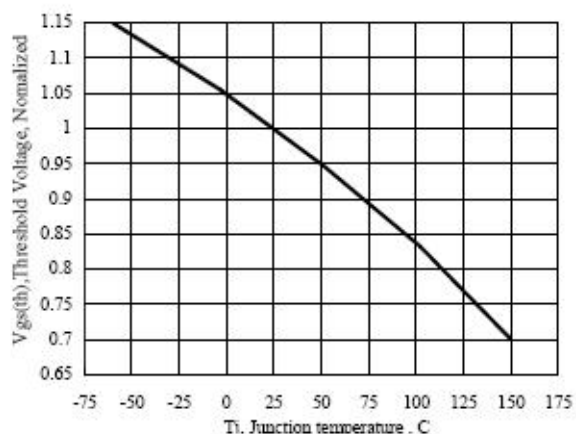


Figure 10 Typical Theshold Voltage vs Junction Temperature

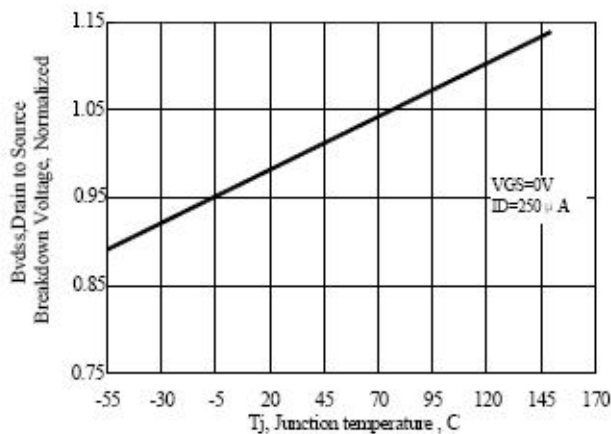


Figure 11 Typical Breakdown Voltage vs Junction Temperature

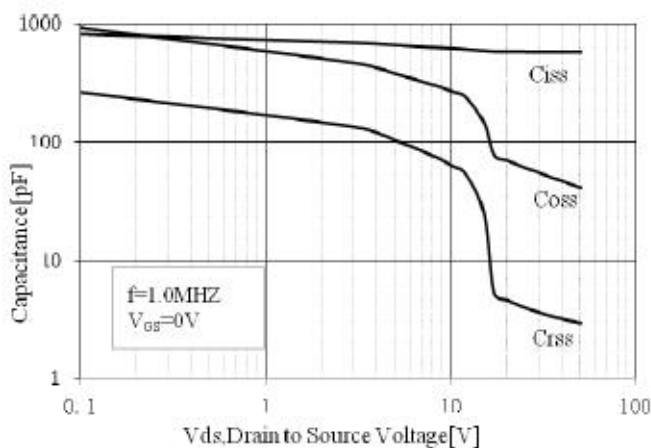


Figure 12 Typical Capacitance vs Drain to Source Voltage

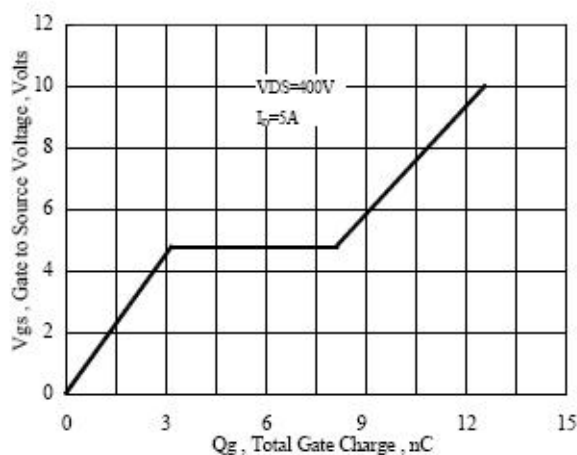


Figure 13 Typical Gate Charge vs Gate to Source Voltage