



GL64N60A64FD

Silicon N-Channel Power MOSFET Integrated FRD

General Description:

GL64N60A64FD, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit . The package form is TO-264, which accords with the RoHS standard.

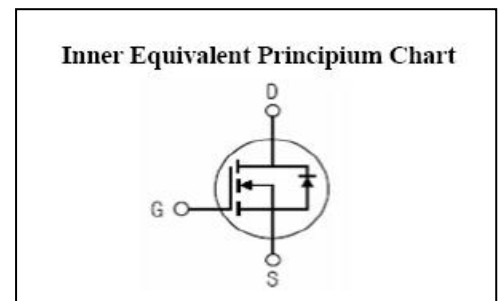
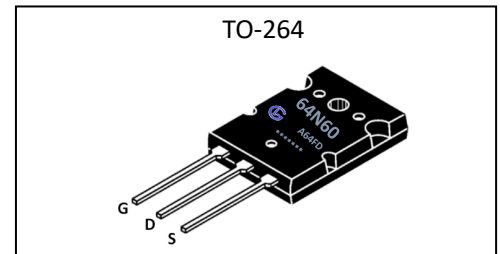
Features:

- Fast Switching
- Low ON Resistance
- Low Gate Charge Minimize Switching loss
- Fast Recovery Body Diode
- 100% Single Pulse avalanche energy Test

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

V_{DSS}	600	V
I_D	64	A
$P_D(T_C=25^{\circ}C)$	1040	W
$R_{DS(ON)type}$	80	m Ω



Absolute (Tc= 25°C unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	64	A
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	150	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy	3500	mJ
dv/dt	Peak Diode Recovery dv/dt	20	V/ns
P_D	Power Dissipation	1040	W
	Derating Factor above 25°C	8.32	W/°C
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T_L	Maximum Temperature for Soldering	300	°C
T_{PAK}	Leads at 0.63 in(1.6mm) from Case for 10S, Package Body for 10S.	260	

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device



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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	600	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=600V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	25	μA
		$V_{DS}=480V, V_{GS}=0V, T_a=125^\circ\text{C}$	--	--	500	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	200	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-200	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=32A$	--	80	95	$m\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=8mA$	3.0	--	5.0	V
g_{fs}	Forward Transconductance	$V_{DS}=20V, I_D=32A$	40	--	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	12000	--	pF
C_{oss}	Output Capacitance		--	1150	--	
C_{rss}	Reverse Transfer Capacitance		--	80	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=32A, V_{DD}=300V$ $V_{GS}=10V, R_g=1\Omega$	--	28	--	ns
t_r	Rise Time		--	23	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	79	--	
t_f	Fall Time		--	24	--	
Q_g	Total Gate Charge	$I_D=32A, V_{DD}=300V$ $V_{GS}=10V$	--	200	--	nC
Q_{gs}	Gate to Source Charge		--	70	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	68	--	



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Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	64	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	150	A
V_{SD}	Diode Forward Voltage	$I_S=64A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=50A, T_J=25^{\circ}C$	--	145	200	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s, V_R=100V$	--	0.6	--	μC

*Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.12	$^{\circ}C/W$



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Characteristics Curve:

Fig. 1. Output Characteristics
@ 25°C

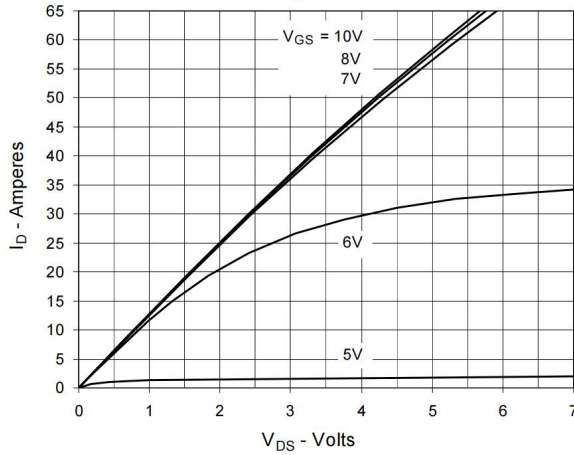


Fig. 2. Extended Output Characteristics
@ 25°C

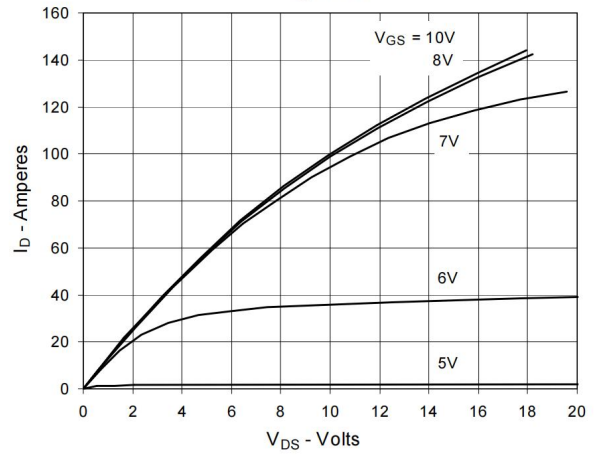


Fig. 3. Output Characteristics
@ 125°C

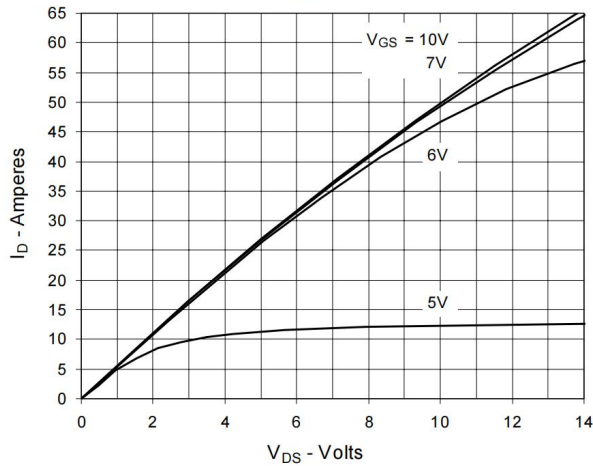


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 32\text{A}$ vs.
Junction Temperature

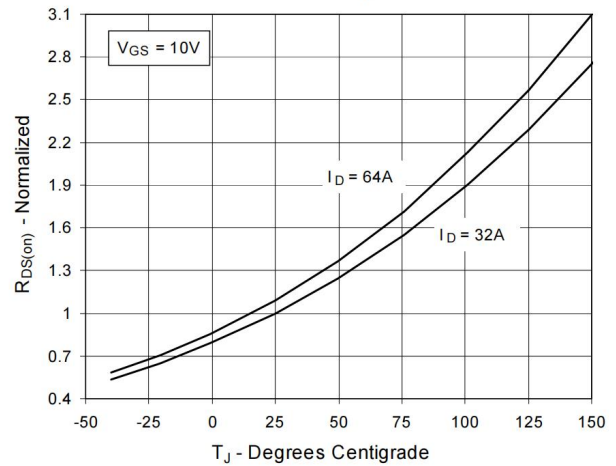


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 32\text{A}$ vs.
Drain Current

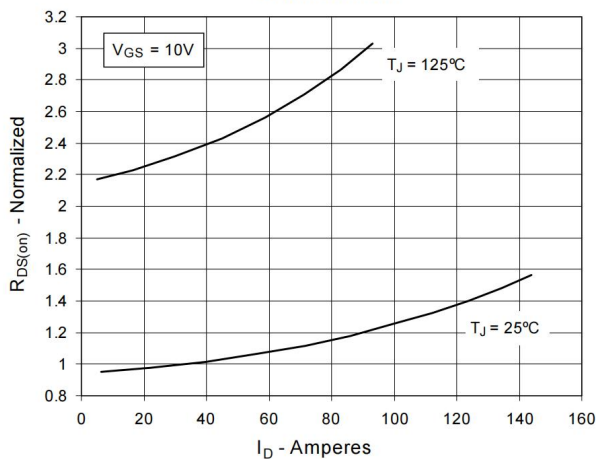
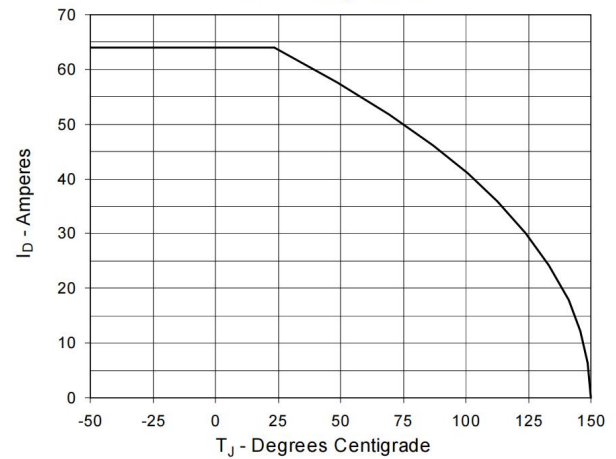


Fig. 6. Maximum Drain Current vs.
Case Temperature





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Fig. 7. Input Admittance

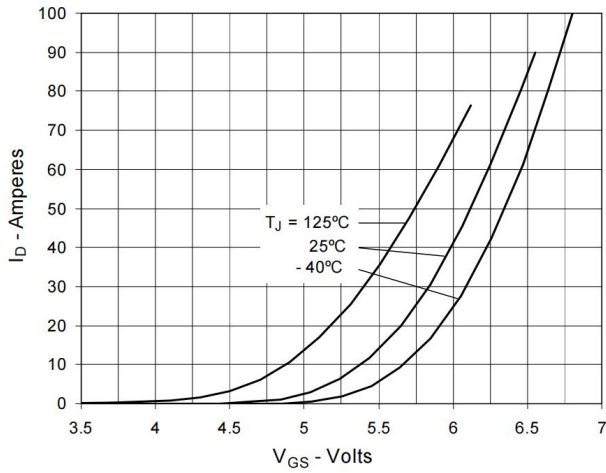


Fig. 8. Transconductance

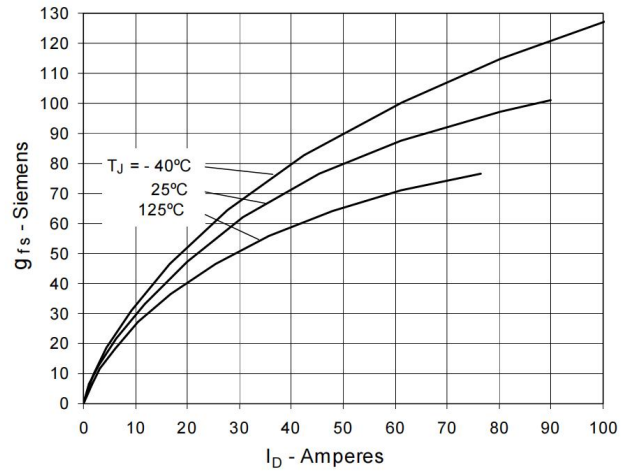


Fig. 9. Forward Voltage Drop of Intrinsic Diode

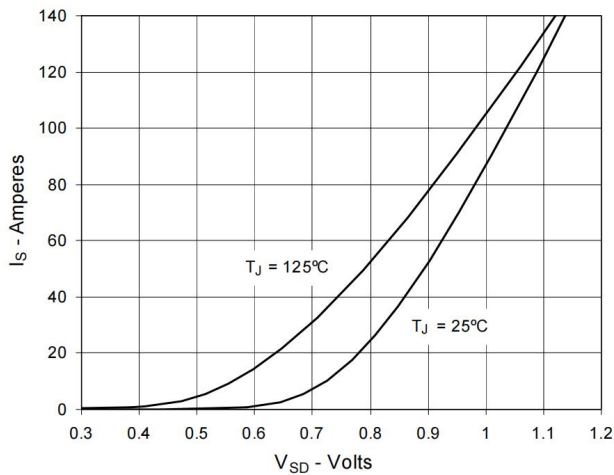


Fig. 10. Gate Charge

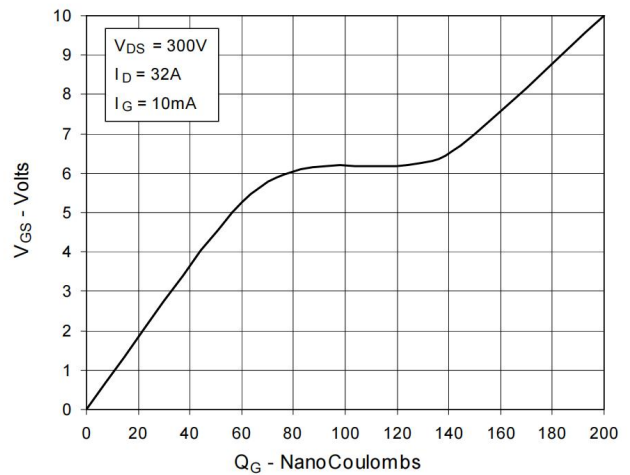


Fig. 11. Capacitance

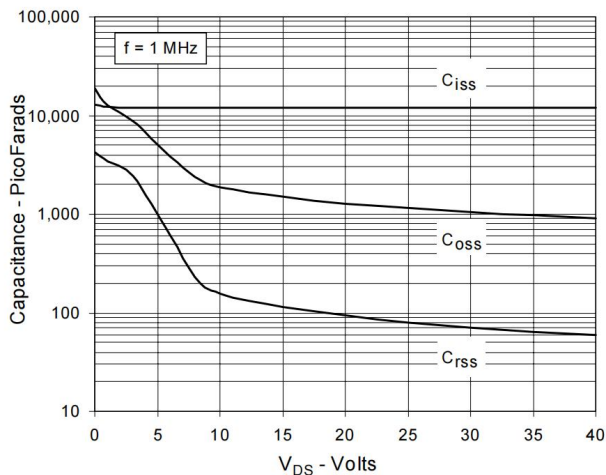


Fig. 12. Forward-Bias Safe Operating Area

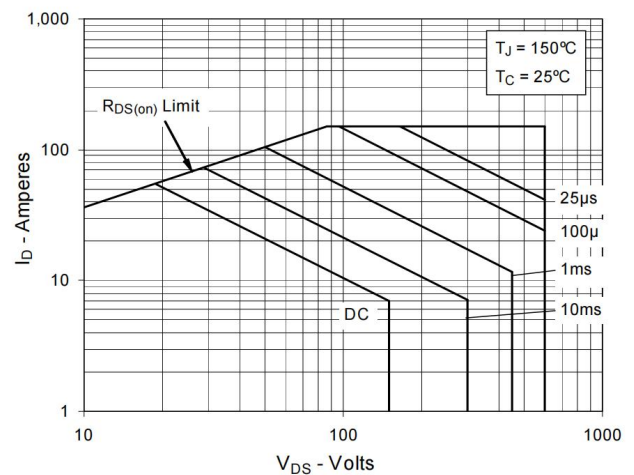


Fig. 13. Maximum Transient Thermal Resistance