GL12N65A0R

GL Silicon N-Channel Power MOSFET

$V_{DSS}(T_C=25℃)$	650	V
I_D	12	A
$P_D(T_C=25℃)$	150	W
$R_{DS(ON)}$	0.58	Ω

General Description:

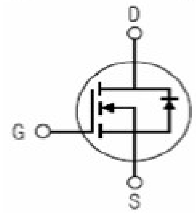
GL12N65A0R, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-263, which accords with the RoHS standard.

TO-263

Features:

- Fast Switching
- ESD Improved Capability
- Low ON Resistance(Typical Data:0.58Ω)
- Low Gate Charge (Typical Data:40nC)
- Low Reverse transfer capacitances(Typical:7.5pF)
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications:

- Power switch circuit of adaptor and charger

Absolute (Tc= 25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	12	A
	Continuous Drain Current T_C = 100 °C	7.5	A
I_{DM} [a1]	Pulsed Drain Current	48	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	900	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	150	W
	Derating Factor above 25°C	1.2	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, –55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics (Tc= 25℃ unless otherwise specified):

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	I_D=250uA,Reference25℃	--	0.68	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS}=650V, V_{GS}=0V,T_a=25℃	--	--	1	μA
		V_{DS}=520V,V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=6A	--	0.58	0.70	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	--	4.0	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V,I_D=6.0A	--	12	--	S
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	2300	--	pF
C_{oss}	Output Capacitance		--	155	--	
C_{rss}	Reverse Transfer Capacitance		--	7.5	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=12.0A,V_{DD}=350V V_{GS}=10V,R_g=10Ω	--	28	--	ns
t_r	Rise Time		--	26	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	64	--	
t_f	Fall Time		--	45	--	
Q_g	Total Gate Charge	I_D=12.0A,V_{DD}=350V V_{GS}=10V	--	40	--	nC
Q_{gs}	Gate to Source Charge		--	10	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	14	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	12	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	48	A
V_{SD}	Diode Forward Voltage	I_S=12.0A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=12.0A,T_j=25℃ dI_F/dt=100A/us,V_{GS}=0V	--	320	--	ns
Q_{rr}	Reverse Recovery Charge		--	3500	--	nC
Pulse width tp≤380μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	0.83	℃/W
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10.0mH, I_D=14.5A, Start T_J=25℃
[a3]: I_{SD} =12A,di/dt≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve:

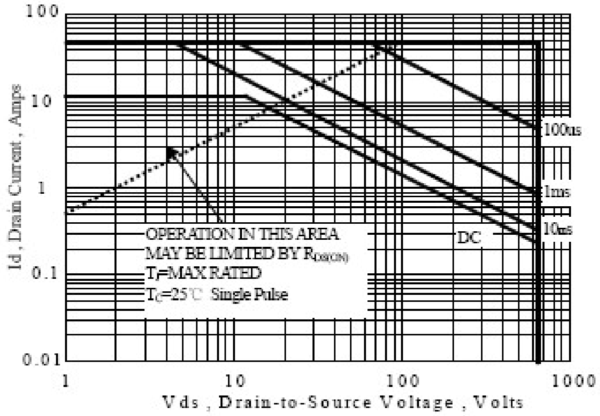


Figure 1 Maximum Forward Bias Safe Operating Area

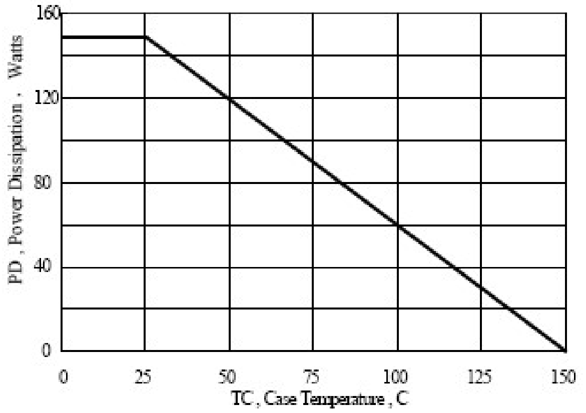


Figure 2 Maximum Power Dissipation vs Case Temperature

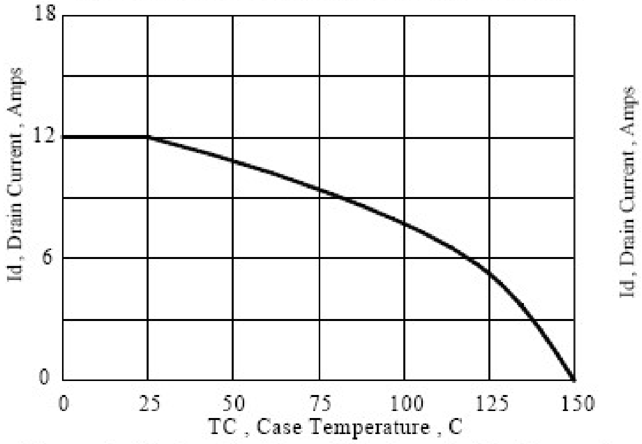


Figure 3 Maximum Continuous Drain Current vs Case Temperature

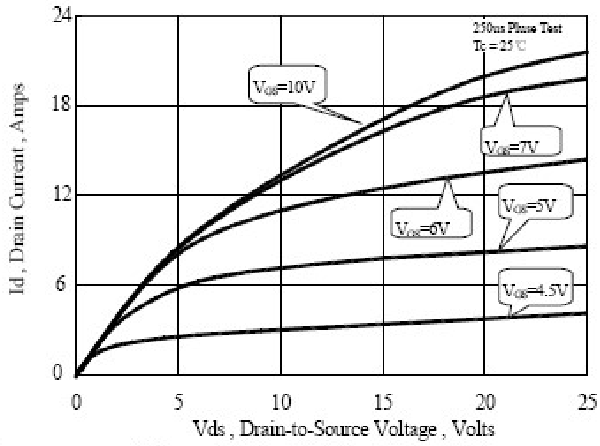


Figure 4 Typical Output Characteristics

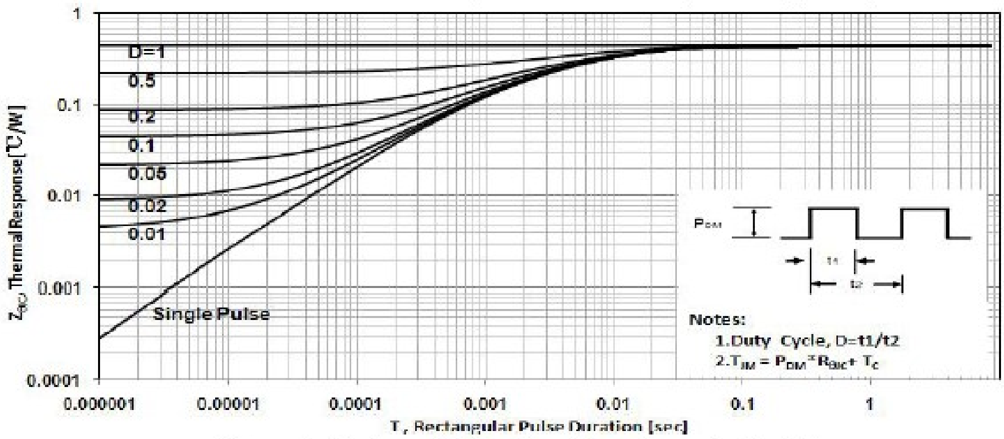


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

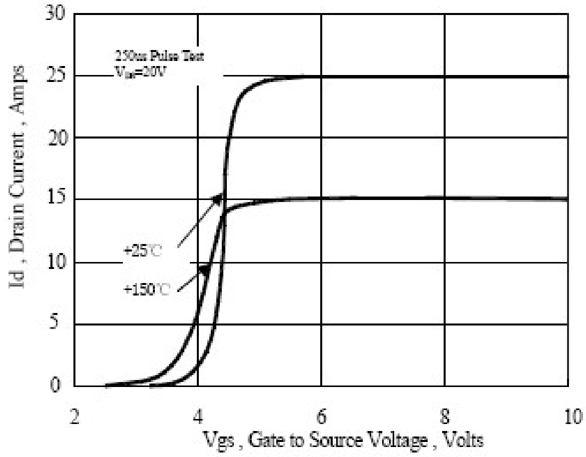


Figure 6 Typical Transfer Characteristics

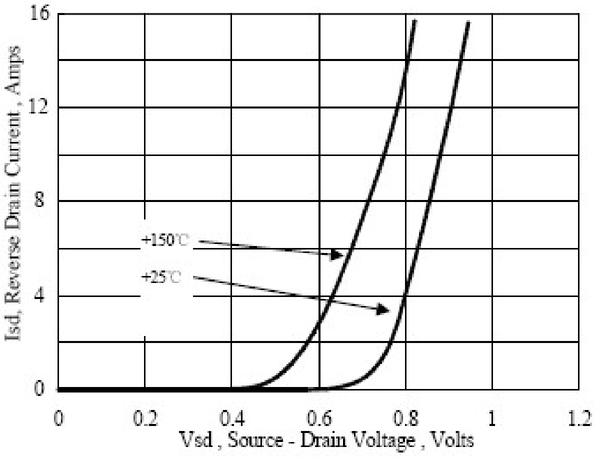


Figure 7 Typical Body Diode Transfer Characteristics

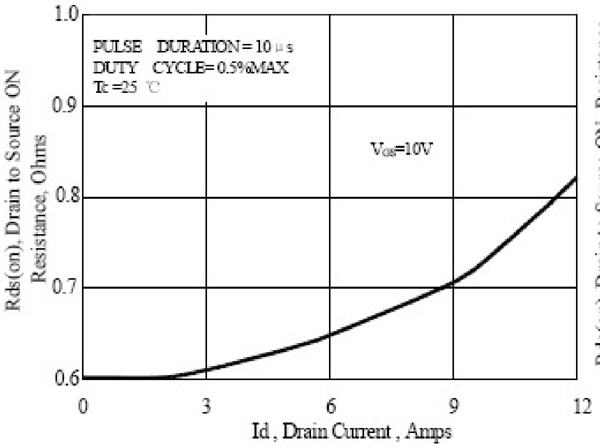


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

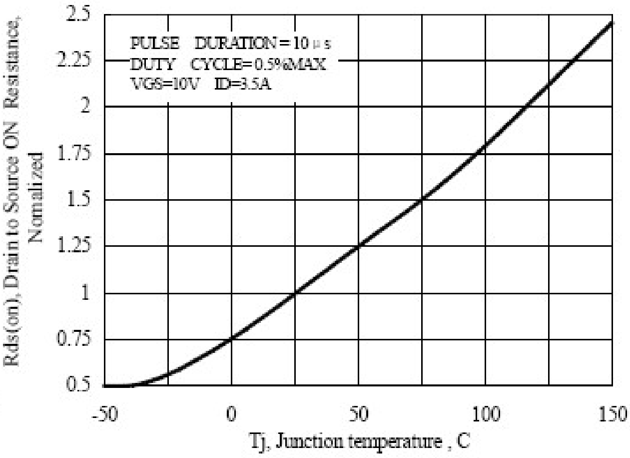


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

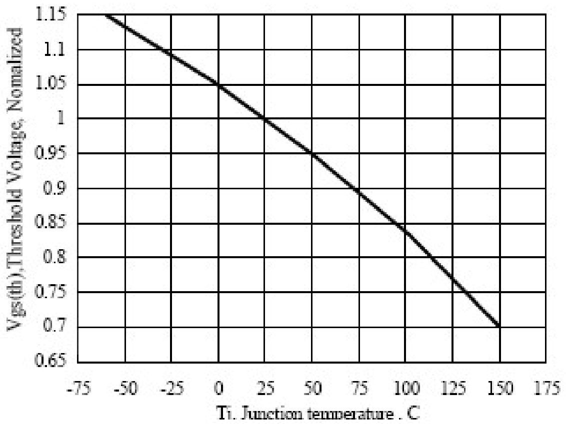


Figure 10 Typical Theshold Voltage vs Junction Temperature

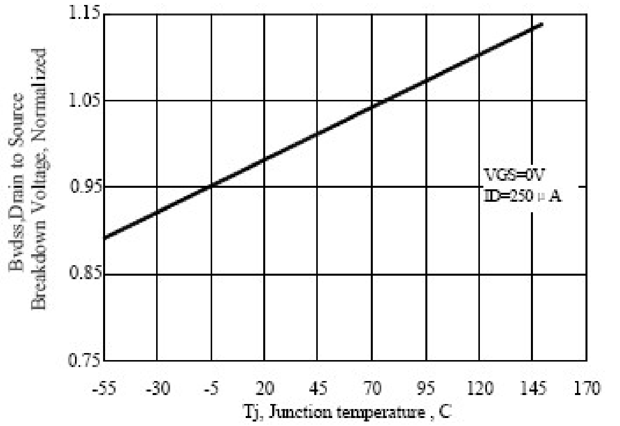


Figure 11 Typical Breakdown Voltage vs Junction Temperature

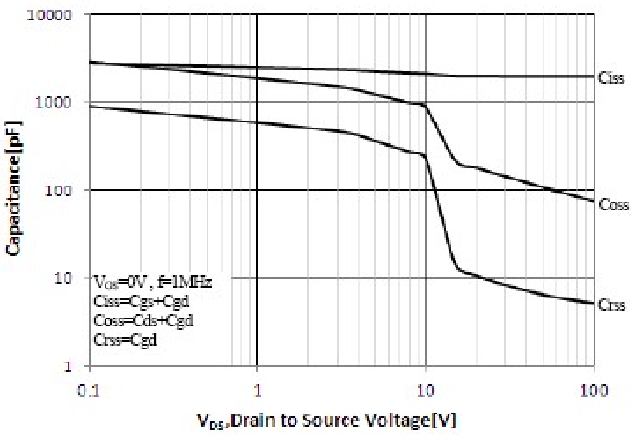


Figure 12 Typical Capacitance vs Drain to Source Voltage

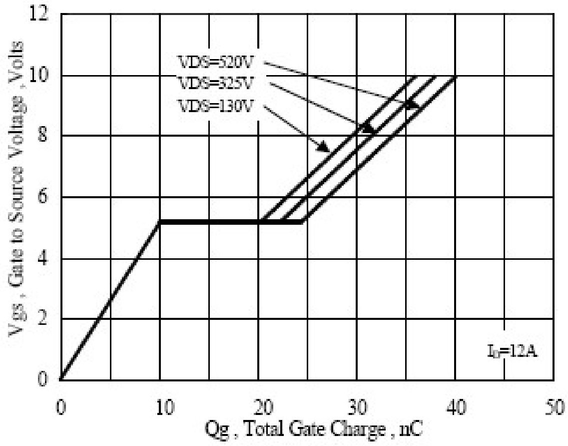


Figure 13 Typical Gate Charge vs Gate to Source Voltage