



GL12N90FA9

Silicon N-Channel Power MOSFET

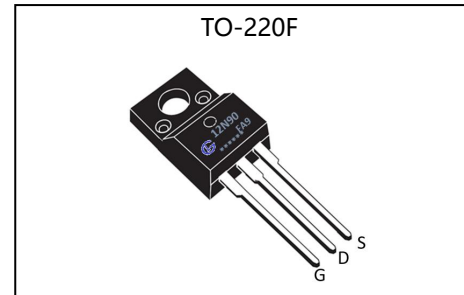
General Description

GL12N90FA9, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

V_{DSS}	900	V
I_D	12	A
$P_D(T_C=25^{\circ}C)$	60	W
$R_{DS(ON),TYP.}$	0.75	Ω

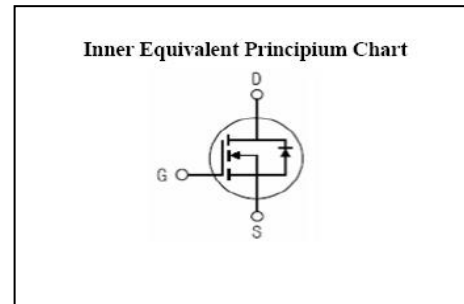
Features

- Fast Switching
- Low ON Resistance($R_{ds(on)} \leq 1.0\Omega$)
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test



Applications

- Power switch circuit of adaptor and charger



Absolute (Tc=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current	12	A
	Continuous Drain Current $T_C=100^{\circ}C$	9.6	A
I_{DM}^{a1}	Pulsed Drain Current	48	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	500	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	60	W
	Derating Factor above 25°C	0.48	W/°C
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T_L	Maximum Temperature for Soldering	300	°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device



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Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.08	°C/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/ W

Electrical Characteristics (Tc= 25°C unless otherwise specified)

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	900	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=900V, V_{GS}=0V, T_a=25^\circ C$	--	--	1	μA
		$V_{DS}=720V, V_{GS}=0V, T_a=125^\circ C$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=6A$	--	0.75	0.9	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=6A$	--	15	--	S

Pulse width<380 μ s; duty cycle<2%.

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	2600	--	pF
C_{oss}	Output Capacitance		--	250	--	
C_{rss}	Reverse Transfer Capacitance		--	50	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=12A, V_{DD}=400V$ $V_{GS}=10V, R_g=4.7\Omega$	--	30	--	ns
t_r	Rise Time		--	20	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	70	--	
t_f	Fall Time		--	20	--	
Q_g	Total Gate Charge	$I_D=12A, V_{DD}=640V$ $V_{GS}=10V$	--	90	--	nC
Q_{gs}	Gate to Source Charge		--	15	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	45	--	



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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	12	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	48	A
V_{SD}	Diode Forward Voltage	$I_S=12A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=12A, T_J=25^{\circ}C$	--	500	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt=100A/\mu s, V_{GS}=0V$	--	6.0	--	μC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $L=10mH$, $I_D=10.0A$, Start $T_J=25^{\circ}C$

a3: $I_{SD}=12A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS}$, Start $T_J=25^{\circ}C$



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Characteristics Curves

Figure 1. Output characteristics

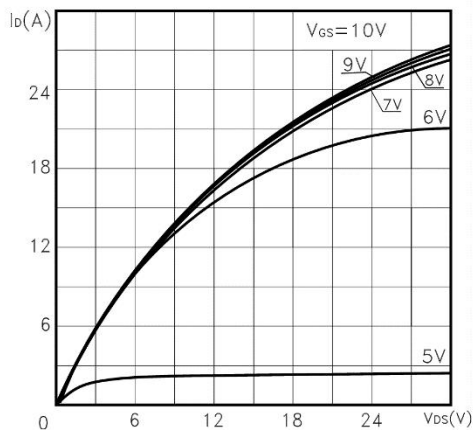


Figure 2. Transfer characteristics

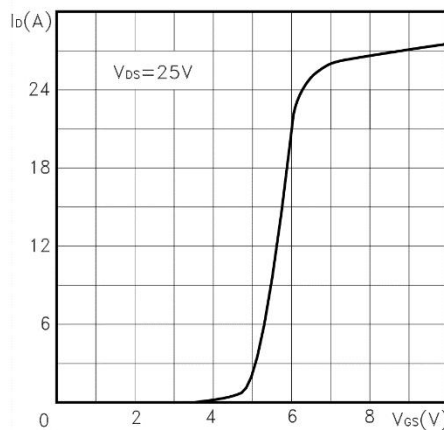


Figure 3. Transconductance

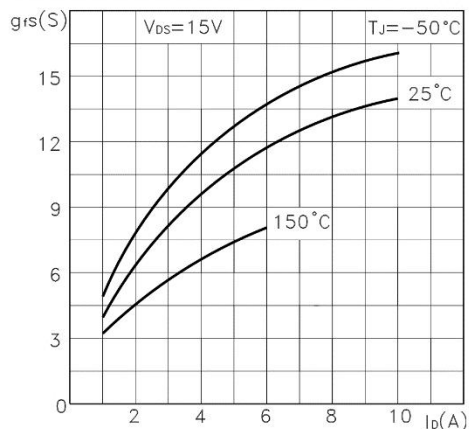


Figure 4. Static drain-source on-resistance

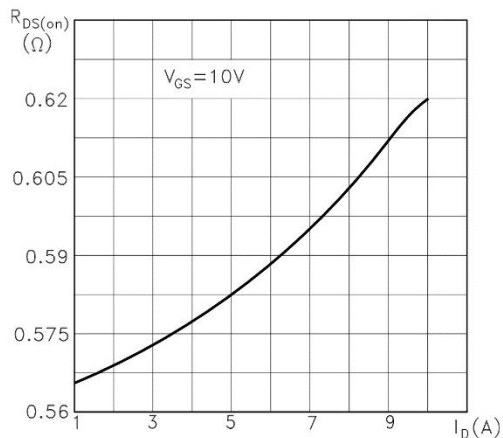


Figure 5. Gate charge vs gate-source voltage

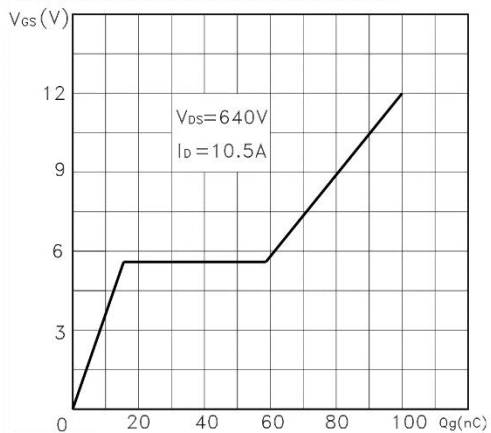


Figure 6. Capacitance variations

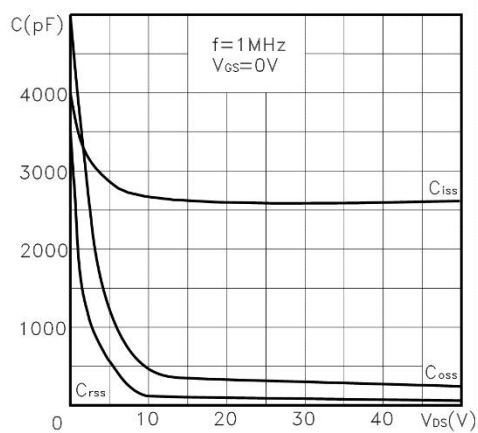


Figure 7. Normalized gate threshold voltage vs temperature

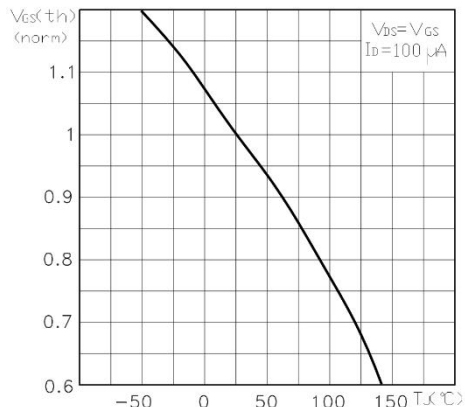


Figure 8. Normalized on-resistance vs temperature

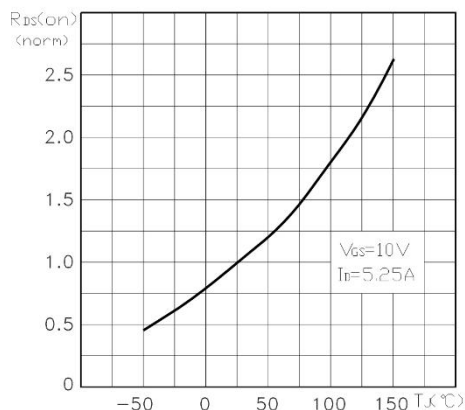


Figure 9. Source-drain diode forward characteristics

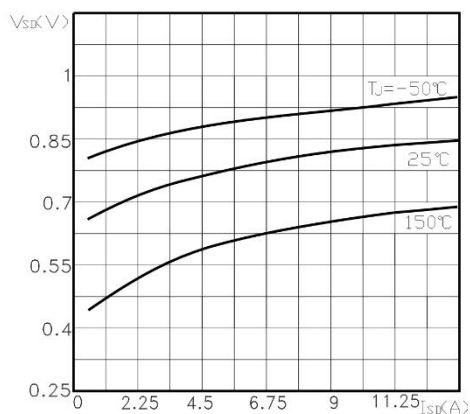


Figure 10. Normalized BV_{DSS} vs temperature

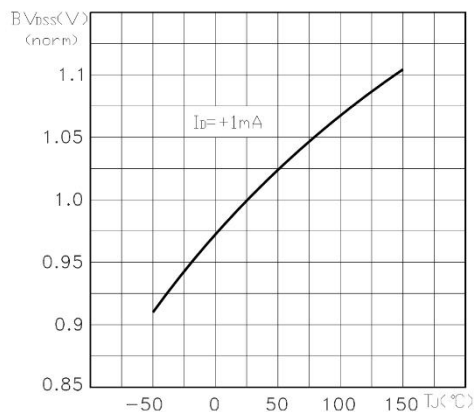


Figure 11. Safe operating area

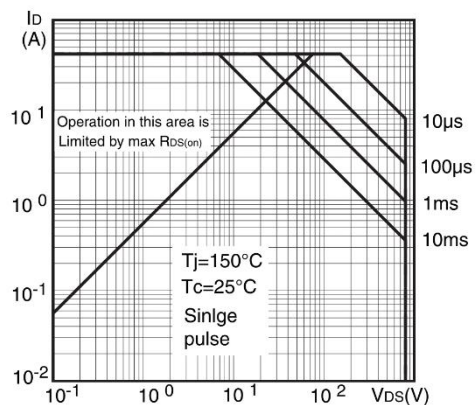


Figure 12. Thermal impedance

