

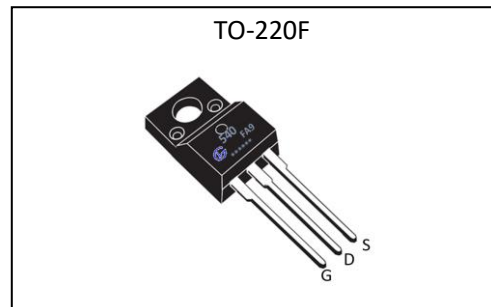
General Description:

The CS540FA9 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TO-220F, which accords with the RoHS standard.

V_{DSS}	100	V
I_D	30	A
P_D	41	W
$R_{DS(ON)type}$	18	m Ω

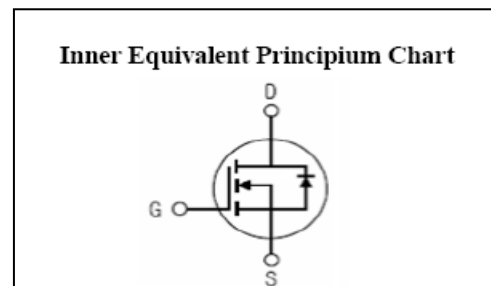
Features:

- $R_{DS(ON)} < 23m\Omega$ @ $V_{GS}=10V$ (Typ18m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications:

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Absolute ($T_c = 25^\circ C$ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	30	A
I_{DM}	Pulsed Drain Current	70	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	41	W
E_{AS}	Single pulse avalanche energy ^{a5}	120	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range	175, -55 to 175	$^\circ C$



GL540FA9

GL Silicon N-Channel Power MOSFET

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=100V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-0.1	μA

ON Characteristics^{a3}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=10A$	--	18	238	m Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	--	2.5	V

Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$

Dynamic Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	--	15	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0\text{MHz}$	--	989	--	pF
C_{oss}	Output Capacitance		--	58	--	
C_{rss}	Reverse Transfer Capacitance		--	61	--	

Resistive Switching Characteristics^{a4}

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=50V, R_L=5\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	--	4	--	ns
t_r	Rise Time		--	3	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	12	--	
t_f	Fall Time		--	4	--	
Q_g	Total Gate Charge	$V_{DD}=50V, I_D=15A$ $V_{GS}=10V$	--	18	--	nC
Q_{gs}	Gate to Source Charge		--	4	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	5	--	

GL Silicon N-Channel Power MOSFET

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	30	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S = 15A, V_{GS} = 0V$	--	--	1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case ^{a2}	3.7	°C/W

^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2}: Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

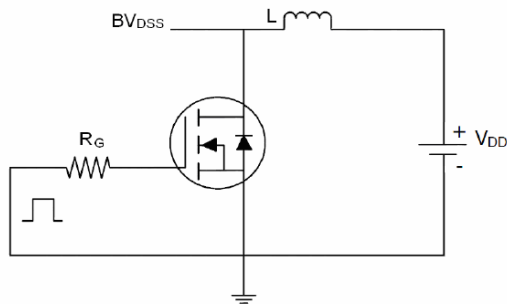
^{a3}: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

^{a4}: Guaranteed by design, not subject to production

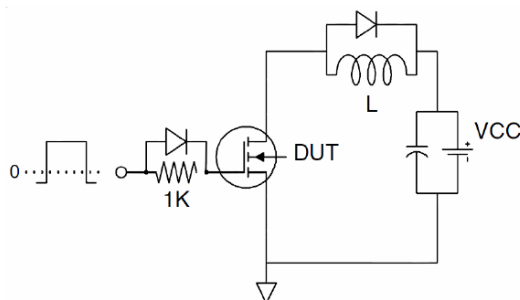
^{a5}: EAS condition: $T_j = 25^\circ\text{C}, V_{DD} = 50V, V_G = 10V, L = 0.5\text{mH}, R_g = 25\Omega, I_{AS} = 32A$

Test circuit

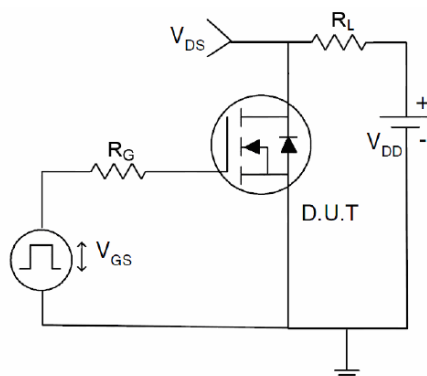
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Characteristics Curve:

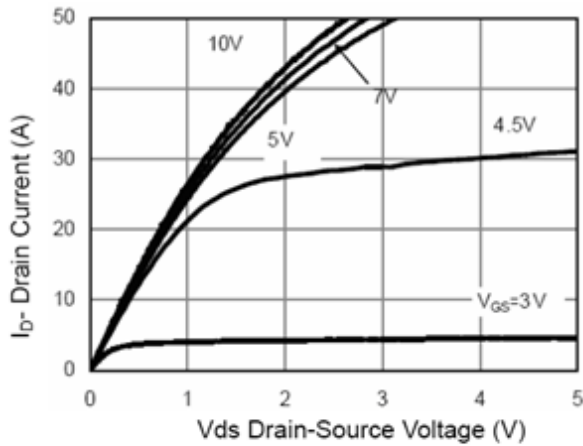


Figure 1 Output Characteristics

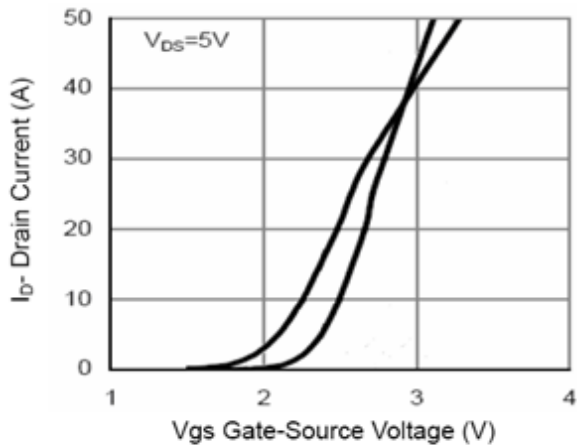


Figure 2 Transfer Characteristics

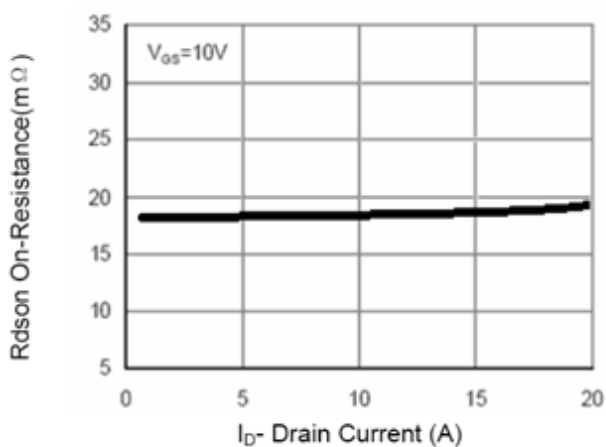


Figure 3 Rdson- Drain Current

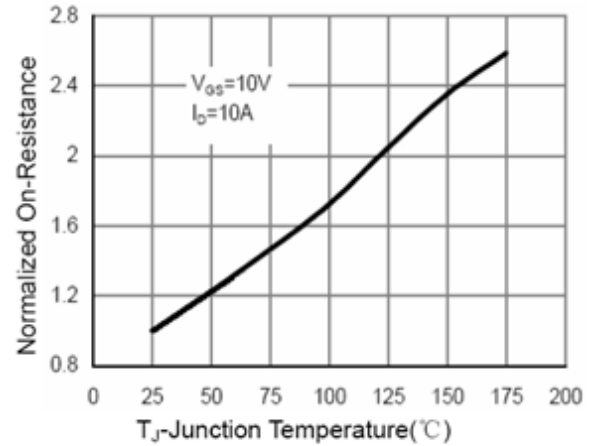


Figure 4 Rdson-Junction Temperature

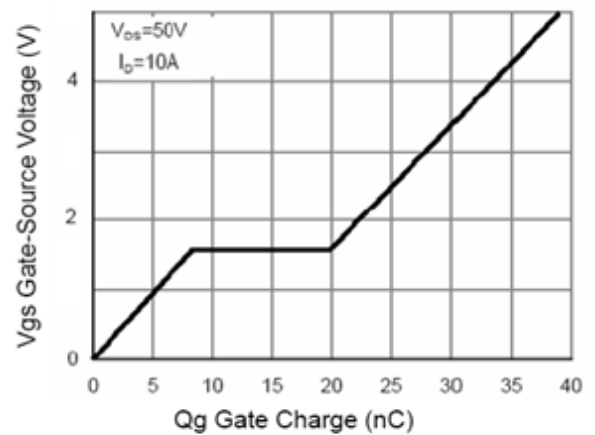


Figure 5 Gate Charge

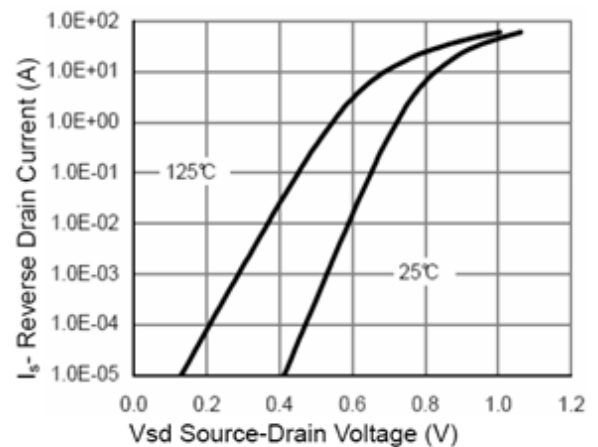


Figure 6 Source- Drain Diode Forward

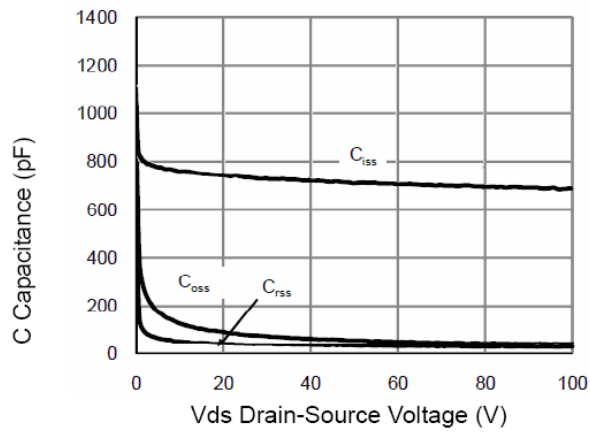


Figure 7 Capacitance vs Vds

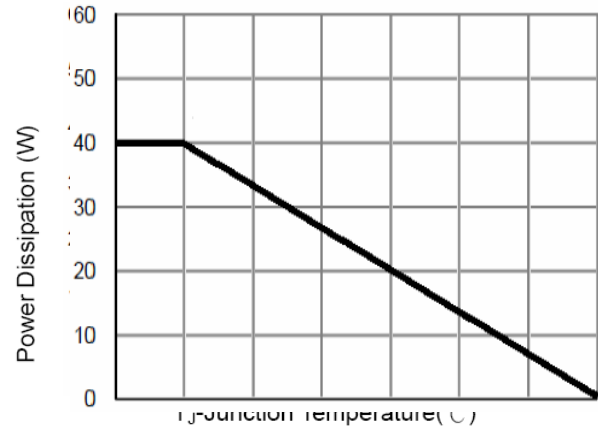


Figure 9 Power De-rating

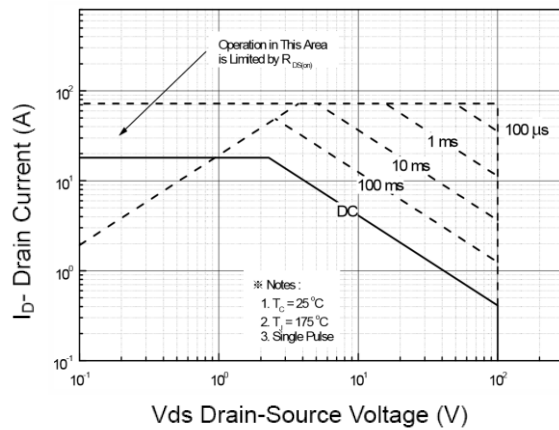


Figure 8 Safe Operation Area

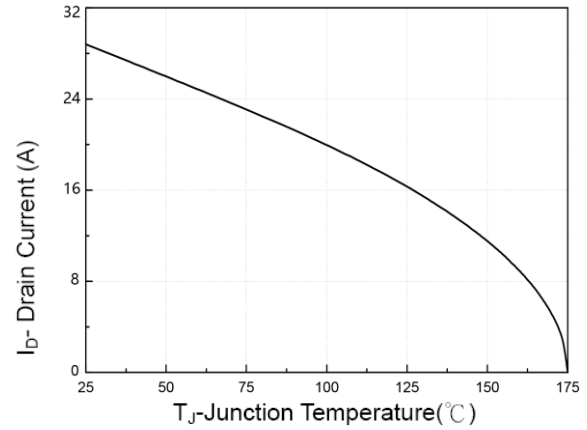


Figure 10 Current De-rating

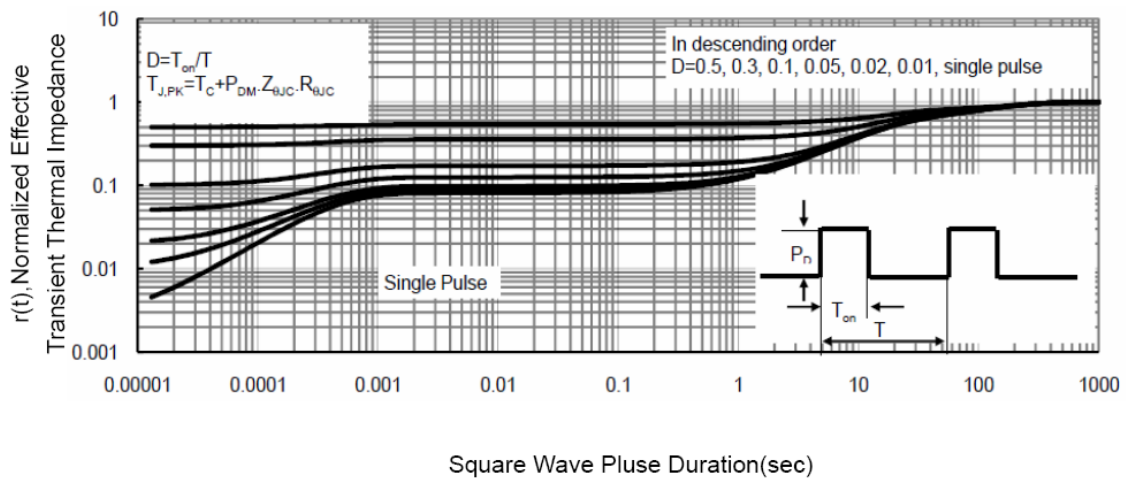


Figure 11 Normalized Maximum Transient Thermal Impedance