



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

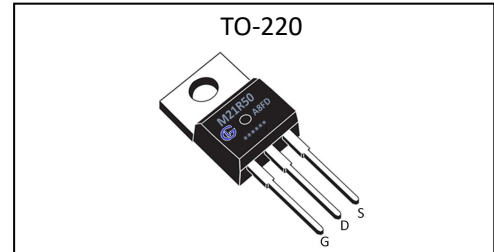
### General Description

GLM21R50A8FD, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220, which accords with the RoHS standard.

$V_{DSS}(T_c=150^{\circ}C)$	500	V
$I_D$	21	A
$P_D(T_c=25^{\circ}C)$	230	W
$R_{DS(ON).type.}$	0.23	$\Omega$

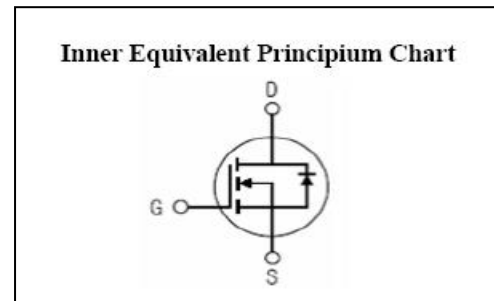
### Features

- Fast Switching
- Low ON Resistance(Typical Data:0.23 $\Omega$ )
- Low Gate Charge Minimize Switching loss
- Fast Recovery Body Diode
- 100% Single Pulse avalanche energy Test



### Applications

- Adaptor
- BLCD Motor
- SMPS Standby Power



### Absolute (Tc=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-to-Source Voltage*1	500	V
$I_D$	Continuous Drain Current	21	A
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V^{*2}$	84	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy	1500	mJ
$I_{AS}$	Avalanche Current	6.8	A
dv/dt	Peak Diode Recovery dv/dt*3	5.0	V/ns
$P_D$	Power Dissipation	230	W
	Derating Factor above 25°C	1.84	W/°C
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	150,-55 to 150	°C
$T_L$	Maximum Temperature for Soldering	300	°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

### Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.54	°C/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	°C/ W



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$V_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	500	--	--	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS}=500V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1.0	$\mu A$
		$V_{DS}=400V, V_{GS}=0V, T_a=125^\circ\text{C}$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance*4	$V_{GS}=10V, I_D=10.5A$	--	0.23	0.28	$\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	3.0	--	5.0	V
$g_{fs}$	Forward Transconductance*4	$V_{DS}=15V, I_D=10.5A$	--	17	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	2864	--	$\mu F$
$C_{oss}$	Output Capacitance		--	286	--	
$C_{rss}$	Reverse Transfer Capacitance		--	25	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=21A, V_{DD}=250V$ $V_{GS}=10V, R_g=25\Omega$	--	33	--	ns
$t_r$	Rise Time		--	75	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	181	--	
$t_f$	Fall Time		--	83	--	
$Q_g$	Total Gate Charge	$I_D=21A, V_{DD}=250V$ $V_{GS}=10V$	--	63	--	nC
$Q_{gs}$	Gate to Source Charge		--	14	--	
$Q_{gd}$	Gate to Drain ( "Miller" )Charge		--	24	--	



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$I_{SD}$	Continuous Source Current (Body Diode)		--	--	21	A
$I_{SM}$	Maximum Pulsed Current (Body Diode)		--	--	80	A
$V_{SD}$	Diode Forward Voltage	$I_S=21A, V_{GS}=0V$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_S=21A, T_j=25^\circ C$	--	105	200	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt=100A/\mu s, V_{GS}=0V$	--	316	--	nC

\*1:  $T_j = +25^\circ C$  to  $+150^\circ C$

\*2: Repetitive rating; pulse width limited by maximum junction temperature.

\*3:  $I_{SD}=21A, di/dt < 100A/\mu s, V_{DD} < BV_{DSS}, T_j = +150^\circ C$ .

\*4: Pulse width  $< 380\mu s$ ; duty cycle  $< 2\%$ .



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

### Characteristics Curves

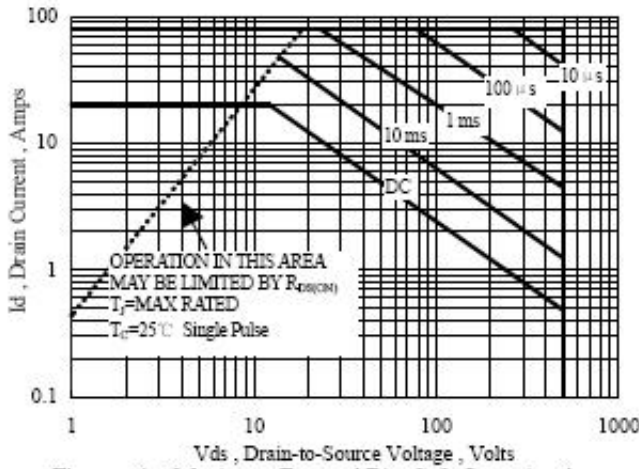


Figure 1 Maximum Forward Bias Safe Operating Area

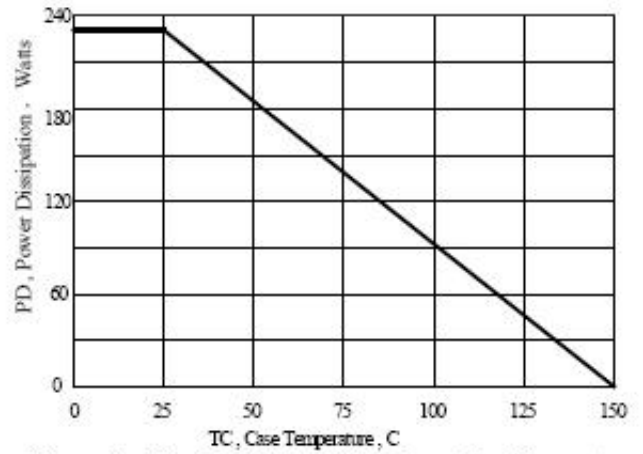


Figure 2 Maximum Power Dissipation vs Case Temperature

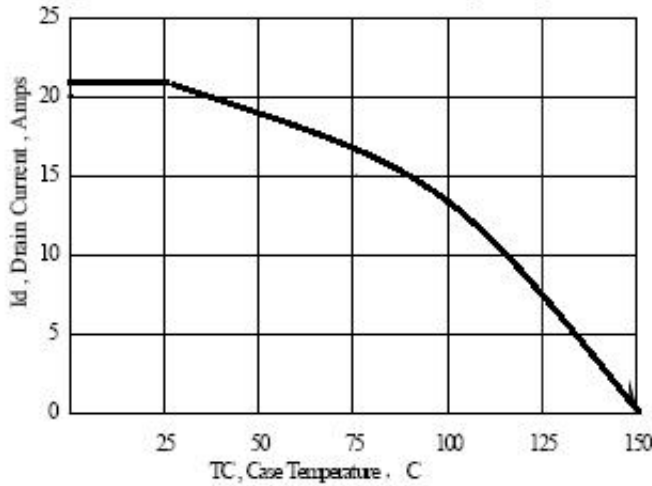


Figure 3 Maximum Continuous Drain Current vs Case Temperature

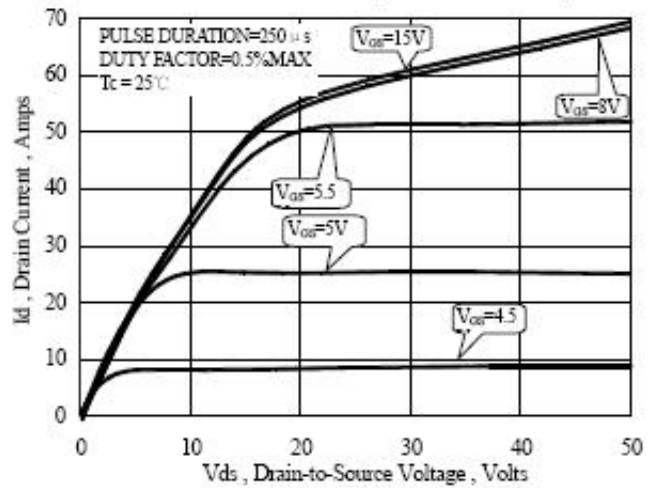


Figure 4 Typical Output Characteristics

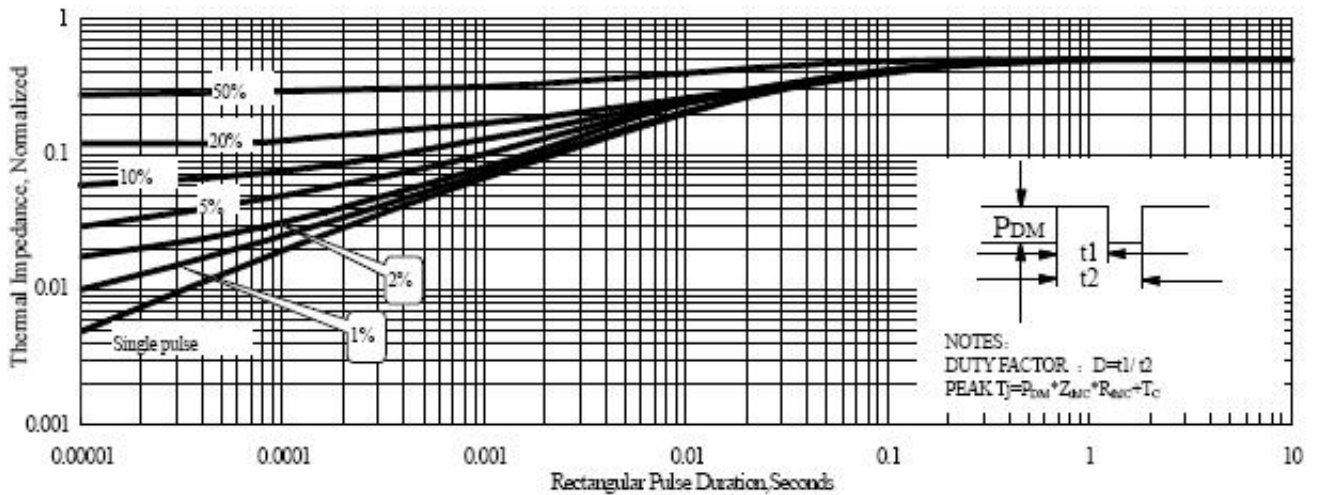


Figure 5 Maximum Effective Thermal Impedance, Junction to Case



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

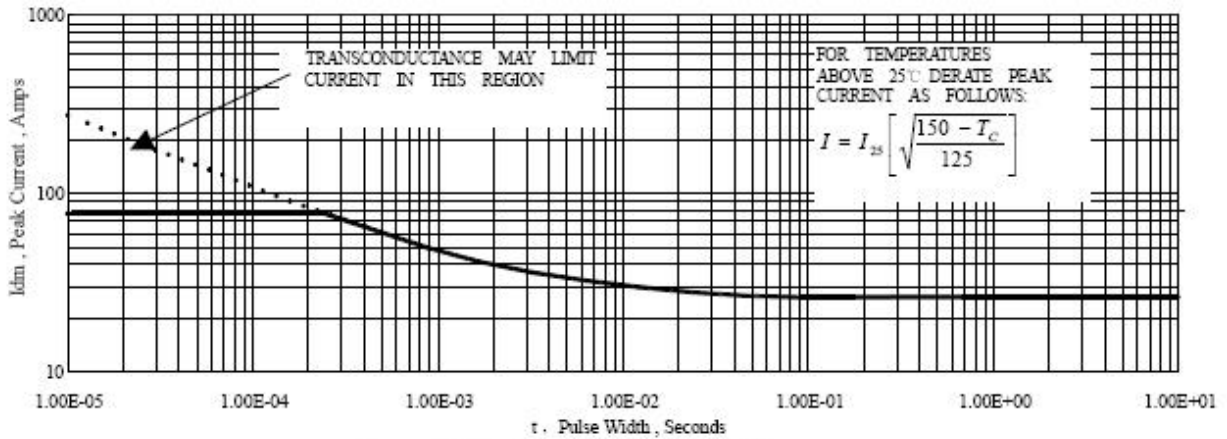


Figure 6 Maximum Peak Current Capability

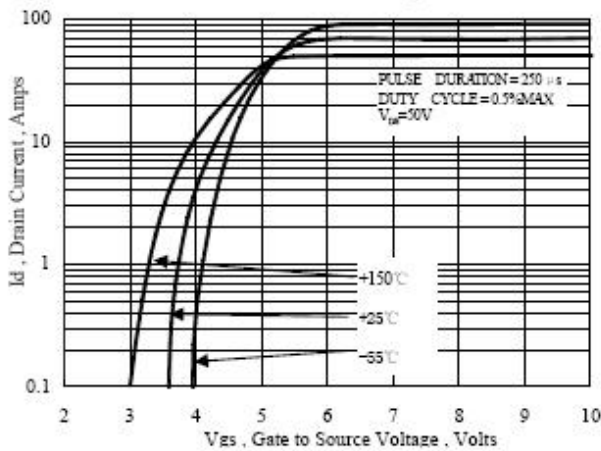


Figure 7 Typical Transfer Characteristics

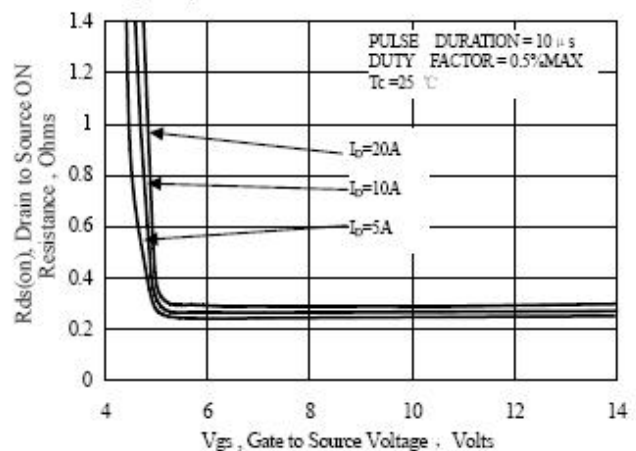


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

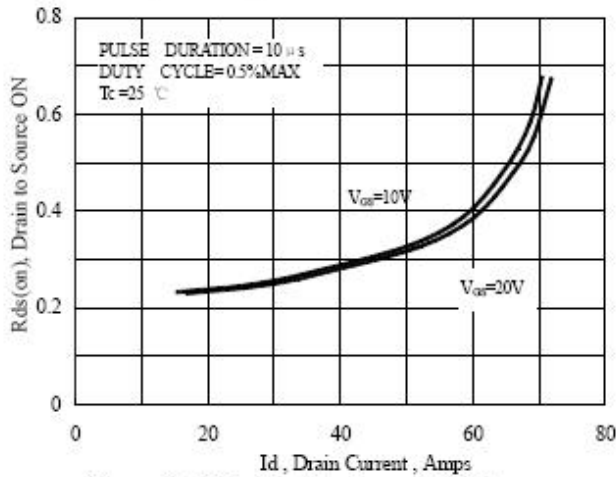


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

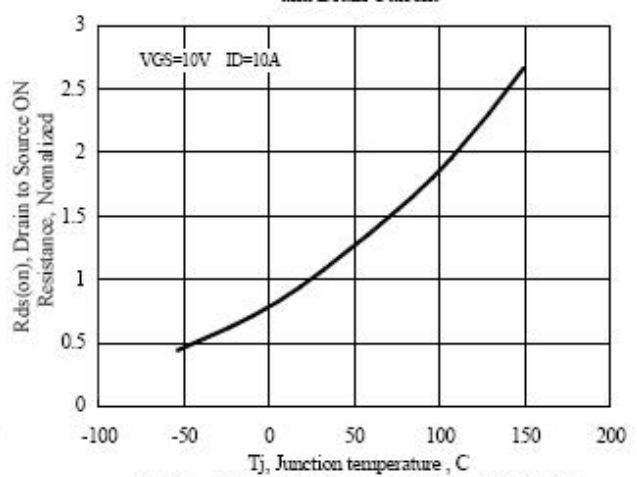


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature



# GL M21R50A8FD

## Silicon N-Channel Power MOSFET Integrated FRD

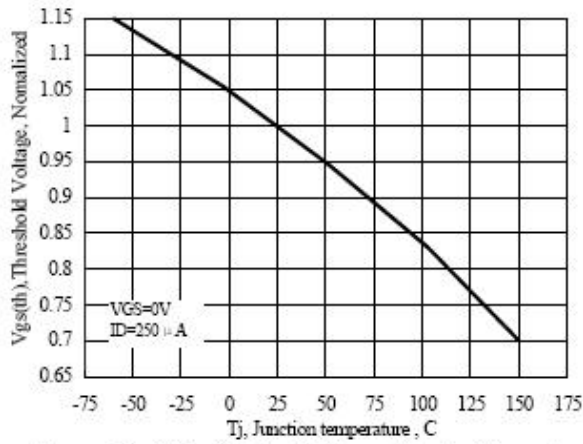


Figure 11 Typical Threshold Voltage vs Junction Temperature

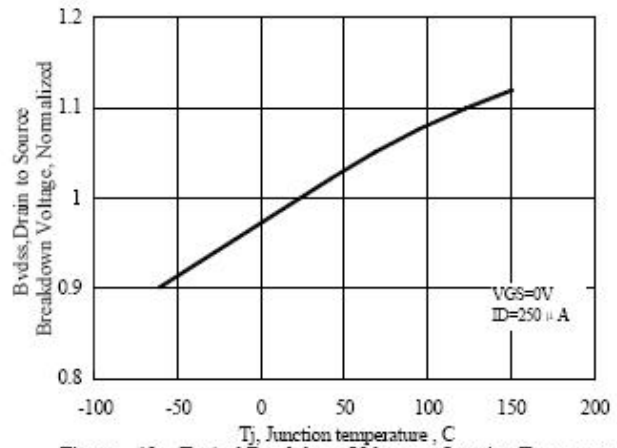


Figure 12 Typical Breakdown Voltage vs Junction Temperature

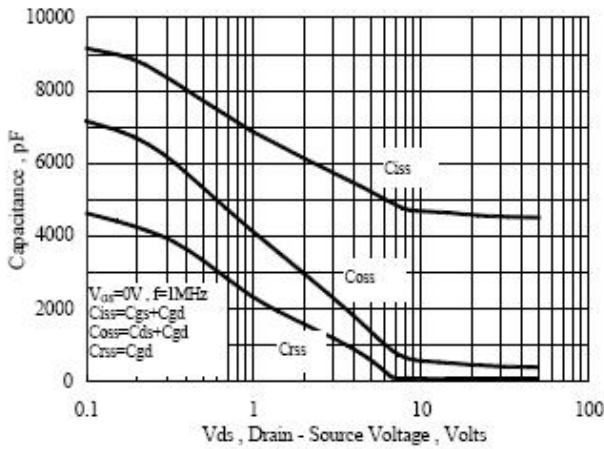


Figure 13 Typical Capacitance vs Drain to Source Voltage

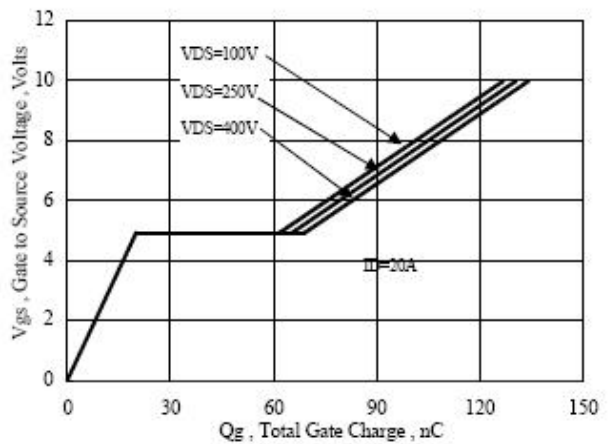


Figure 14 Typical Gate Charge vs Gate to Source Voltage

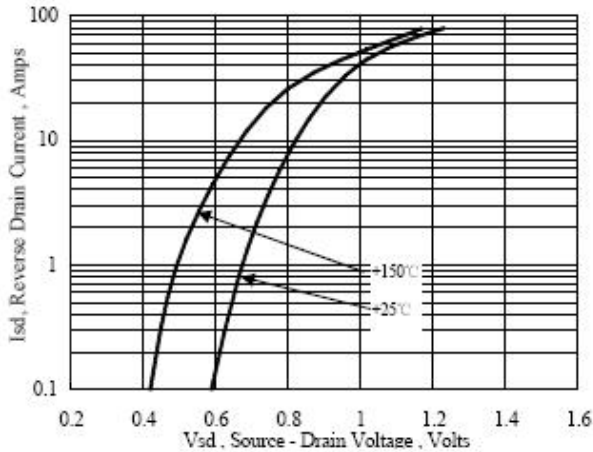


Figure 15 Typical Body Diode Transfer Characteristics

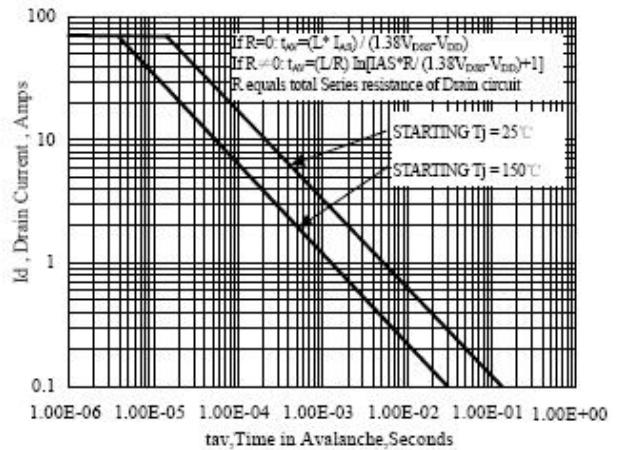


Figure 16 Unclamped Inductive Switching Capability